Operating and Maintenance Manual

Microprocessor Analyzer MPA-1

MOTOROLA

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Part No. 68P20903A01

Operating and Maintenance Manual

Microprocessor Analyzer MPA-1

With Applications Information for:

Motorola M6800, AMI S6800, and other 6800 series,
Motorola EXORcisor™,
Intel 8080(A), AMD 9080, and other 8080 series,
Rockwell PPS-4

MOTOROLA

Printed May, 1976

PRODUCT PERFORMANCE REPORT

NOW Please return this half immediately after the testing or installation of your unit.

In a continuing effort to provide a better product, *we need your help.*

DATE _____ SERIAL # R 3 6 4 8 4

MODEL # MPA-1

F.O. # _____

1. Did your unit perform properly? YES ☐ NO ☐

E. Zdunczyk
Performance Verified By

2. Nature of problem?

☐ Frequency ☐ Deviation ☐ Power Output ☐ Quieting ☐ Audio

Other (Please explain) _____

3. How was the problem fixed?

☐ Adjustment/Alignment ☐ Soldered ☐ Replaced Component

(If so) Part Number/Ckt. Sym. _____

Other (please explain) _____

4. Comments, suggestions

Installed By: MSS # _____

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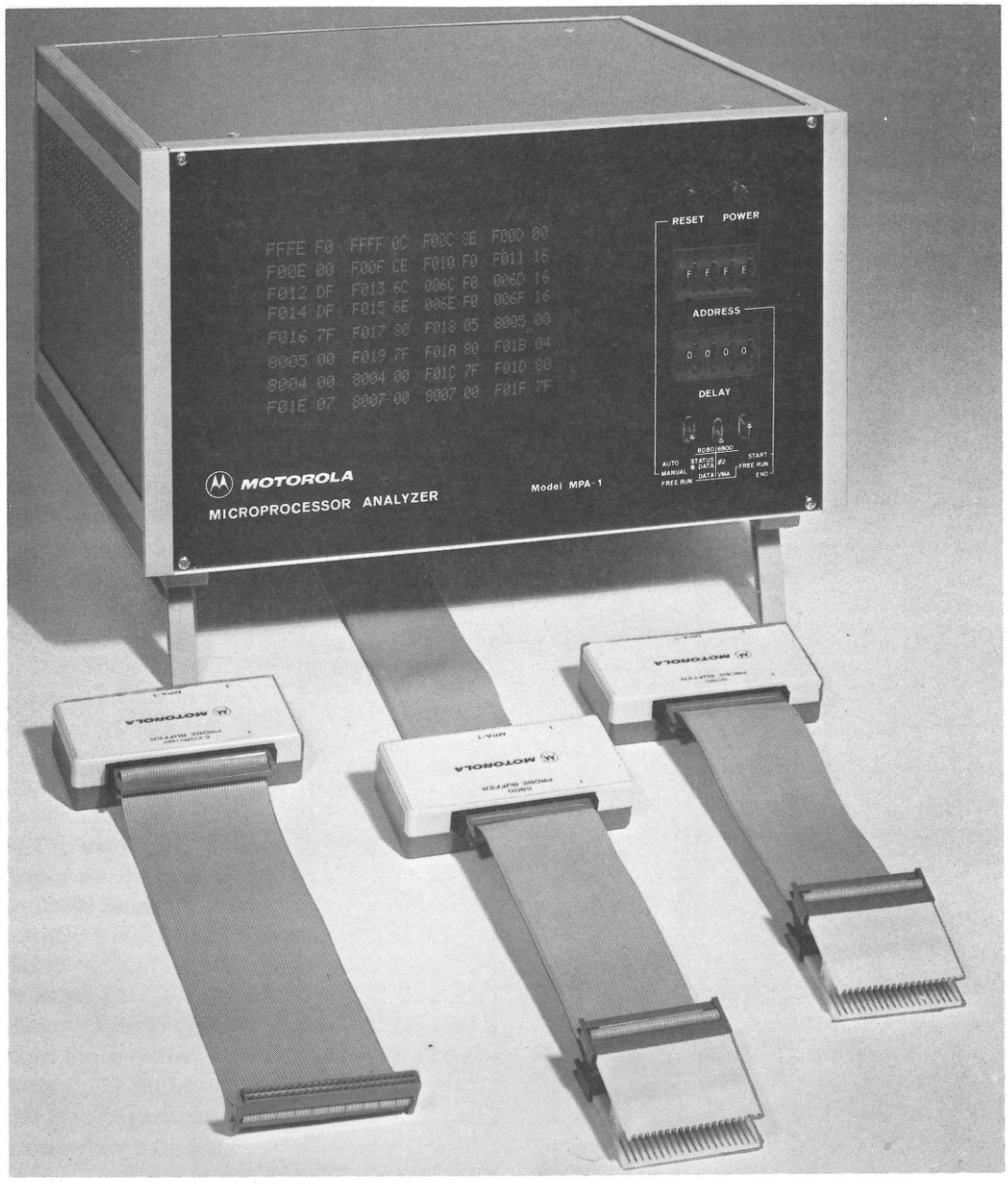


Model MPA—1, Probe Buffers, and Connectors

SECTION 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides operating and maintenance information for the Motorola Model MPA–1 Microprocessor Analyzer. The manual is divided into six sections. Each section describes a specific aspect of MPA–1 operation, applications, or maintenance. All schematic diagrams are located at the rear of the manual in Section 6. The schematics can be folded out for reference while using any other section of the manual. Section 6 also contains block diagrams which summarize the schematics and illustrate the major operating modes of the instrument. Sample programs and operating examples are provided for three generic types of processors: (1) Motorola M6800, (2) Intel 8080, (3) Rockwell PPS–4. Table 1 lists the MPA–1 specifications.

1.2 DESCRIPTION

The basis of MPA–1 operation is word recognition triggering. Using the **ADDRESS** thumbwheel switches on the front panel, a 16-bit trigger word can be set to any location in the address space of the microprocessor. Depending on the mode selected, recognition of the trigger word can either start or end data capture. Use of the **DELAY** thumbwheel switches allows data capture to be delayed up to 65k clock pulses from recognition of the trigger word. When capture is complete, the information is read out on a CRT screen in hexadecimal notation. The output format is similar to a printed page. It is organized into 8 lines of four words each. The rows read from left to right and are ordered from top to bottom of the screen. The 32 words in the display are read out in the order of their execution by the processor.

During data capture, the MPA–1 derives its clock from the microprocessor under test. A front panel switch allows two choices. For the Motorola M6800, Ø2 or the logical product of Ø2 and VMA. For the Intel 8080, the switch allows status bytes to be captured or ignored. When status is captured, it is displayed with corresponding data from 16 locations. Trigger address recognized and buffered clock outputs are available on the back panel for triggering an external counter or oscilloscope.

An external probe buffer is used to connect the MPU under test. CMOS buffers and short lead lengths assure minimal loading of the microprocessor bus. The use of an external probe allows flexibility in interfacing and prevents obsolescence as new processors are introduced.

1.3 UNPACKING–REPACKING

Open the shipping carton and lift out the entire contents – the MPA–1 plus foam inserts. Remove the inserts and plastic cover. Proceed with the Initial Checkout as described in Section 1.6

It is generally advisable to retain the shipping carton and packing materials in case it is necessary to return the unit to the factory or to ship it to any other location. Figure 1 illustrates how to replace the inserts and repack the instrument.

Table 1. Specifications

SIGNAL INPUTS

IMPEDANCE: 10M Ohm shunted by 10 pF (nominal)
LOGIC 0: –0.8 to +0.8 volts
LOGIC 1: 2.3 to 16.0 volts
CLOCK SOURCE: Clock of MPU under test
CLOCK RATE: 2.2 MHz maximum

CLOCK AND TRIGGER OUTPUTS

CLOCK: From clock source, buffered, TTL levels
ADDRESS TRIGGER:
SOURCE: Prompt with address recognition
WIDTH: 200 nSec, TTL levels

DISPLAY

ADDRESS: 4 hexadecimal characters
DATA/STATUS: 2 hexadecimal characters
FORMAT: 8 rows x 4 columns
DIRECTION OF INCREASE: Left to right across rows
SCREEN SIZE: 3" X 5" (9" CRT)
REFRESH RATE: 60 Hz (50 Hz export)

GENERAL

POWER: 105–132V AC, 60 Hz, 60 VA maximum
220V AC, 50 Hz export

DIMENSIONS: HEIGHT: 8.0" (20.3 cm)
WIDTH: 13.0" (33.0 cm)
DEPTH: 12.0" (30.0 cm)

WEIGHT: 24 lbs. (10.9 kg) net
28 lbs. (12.7 kg) shipping

OPERATING TEMPERATURE: 0° C to +45° C

STORAGE TEMPERATURE: –40° C to +65° C

ALTITUDE: 10,000 ft. (3,048 meters) maximum

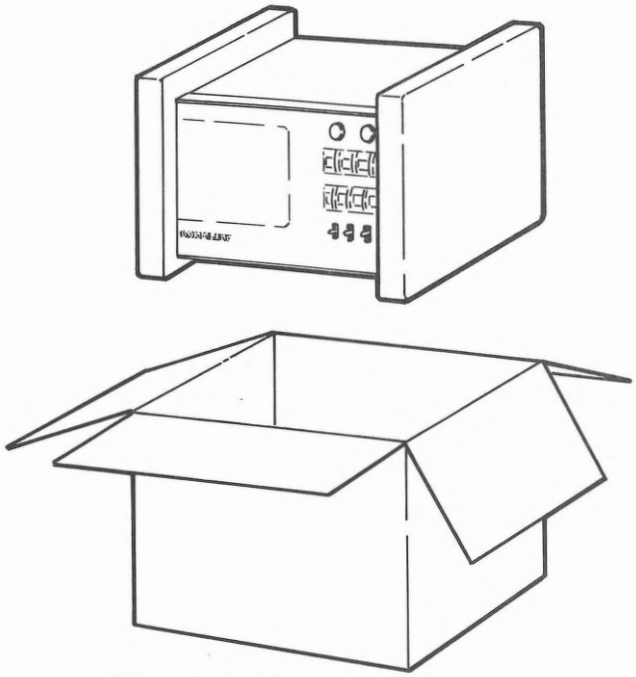


Figure 1. MPA–1 Shipping Carton

1.4 IDENTIFICATION

Figure 2 shows the MPA–1 identification tag which is located on the back panel of the instrument. Refer to this model and serial number in correspondence with Motorola, Inc. or when ordering parts.

REMOVAL OR MUTILATION OF THIS TAG MAY VOID THE WARRANTY OF THIS INSTRUMENT.

MOTOROLA
MODEL NO. MPA–1
SERIAL NO. R0100X

Figure 2. Instrument Identification Tag

1.5 POWER REQUIREMENTS

The power requirements for this instrument are:

105–132V AC, 60 Hz, 60 VA maximum
220V AC, 50 Hz export (See Table 1.)

Any power not meeting these specifications may damage the unit.

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED INSTRUMENT CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS. THE CRT RETAINS A HIGH VOLTAGE CHARGE WHEN THE POWER IS OFF. BEFORE SERVICING, DISCHARGE CRT BY SHORTING THE ANODE CONNECTION TO CHASSIS GROUND (NOT CABINET OR OTHER MOUNTING PARTS). WHEN DISCHARGING . . . GO FROM GROUND TO ANODE WITH A WELL INSULATED PIECE OR WIRE.

1.6 INITIAL CHECKOUT

The Initial Checkout tests much of the MPA–1 circuitry for damage that may have occurred during shipment. A slip included in the shipping carton also describes this procedure. This test should be done promptly on receipt of the instrument to give maximum protection under the warranty.

1. Unpack the MPA–1, and plug the line cord into a power outlet.

2. Set the three-position **AUTO/MANUAL** switch to its lower position – **FREE RUN.**

3. Set the three-position **START/END** switch to its center position – **FREE RUN.**

4. Press the **POWER** switch to turn the instrument on. The indicator should light immediately.

A display with random information similar to Figure 3 should appear in 10–15 seconds. No further activity should appear on the screen. If the indicator does not light, or the display fails to appear, contact Motorola for assistance.

1.7 ACCESSORIES

The following accessories (See Figure 4) are supplied with each MPA–1:

1 – 40-conductor ribbon cable 36 inches long with 40-pin socket connectors at each end.

1 – Probe Buffer. Choice of PB–1, PB–2, PB–3, or PB–4. (See Probe Buffer list below.)

1 – 40-pin IC test clip with 4 inches of ribbon cable.

1 – 40-conductor cable 4 inches long with 40-pin connectors.

1 – 40-conductor cable 8 inches long with 40 individual wire wrap post connectors.

Probe Buffer designations are as follows:

PB–1. Probe Buffer with 40-pin input and output headers factory wire wrapped for Motorola M6800 microprocessor.

PB–2. Probe Buffer with 50-pin input and 40-pin output headers factory wire wrapped to mate with the back panel connector of a Motorola EXORcisor™. Supplied with a 50-conductor cable and 50-pin connectors.

PB–3. Probe Buffer with 40-pin input and output headers factory wire wrapped for Intel 8080 microprocessor.

PB–4. Probe Buffer with 40-pin input and output headers factore wire wrapped for Rockwell PPS–4 microprocessor.

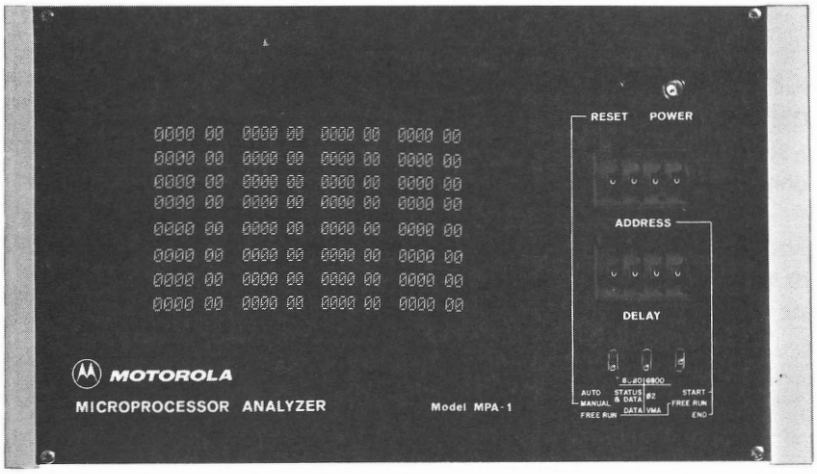


Figure 3. Initial Checkout

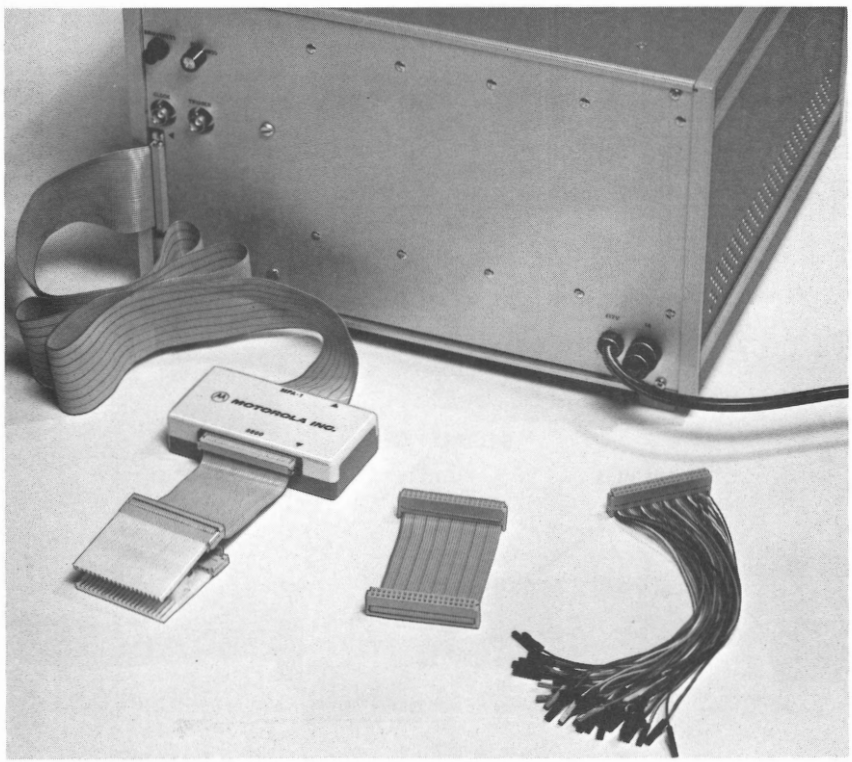


Figure 4. Accessories Supplied

SECTION 2.
OPERATION

2.1 INTRODUCTION

This section explains the more basic aspects of MPA–1 operation: connection to the MPU under test, location, and operation of the controls. Actual operating examples with detailed descriptions of the displays are contained in Section 3.

2.2 CONNECTION TO MPU

Continuity must be maintained between pin 1 of the MPA–1 **INPUT** Connector and pin 1 of the MPU under test. Pin 1 of the **INPUT** Connector and the Probe Buffer are marked with a " ▲ " and a "1", respectively. To aid in making connections, ribbon cables supplied with the instrument have one conductor marked in blue. The following step-by-step procedure will insure proper connections. (See Figure 5.)

1. Connect one end of the 36-inch 40-conductor cable to the **INPUT** Connector of the MPA–1. The blue conductor should be on top and correspond to the ▲ marking.

2. Connect the other end of the 36-inch cable to the output side of the Probe Buffer which is marked **MPA–1.** The blue conductor should correspond to pin 1.

3. The input side of the Probe Buffer is designated by the processor type: **M6800, EXORcisor, 8800,** or **PPS–4.** Attach the test clip, 40, or 50-conductor cable so that the blue conductor corresponds to pin 1.

4a. If connection will be made with the 40-pin test clip, determine which end of the MPU package has pin 1 and connect the test clip accordingly.

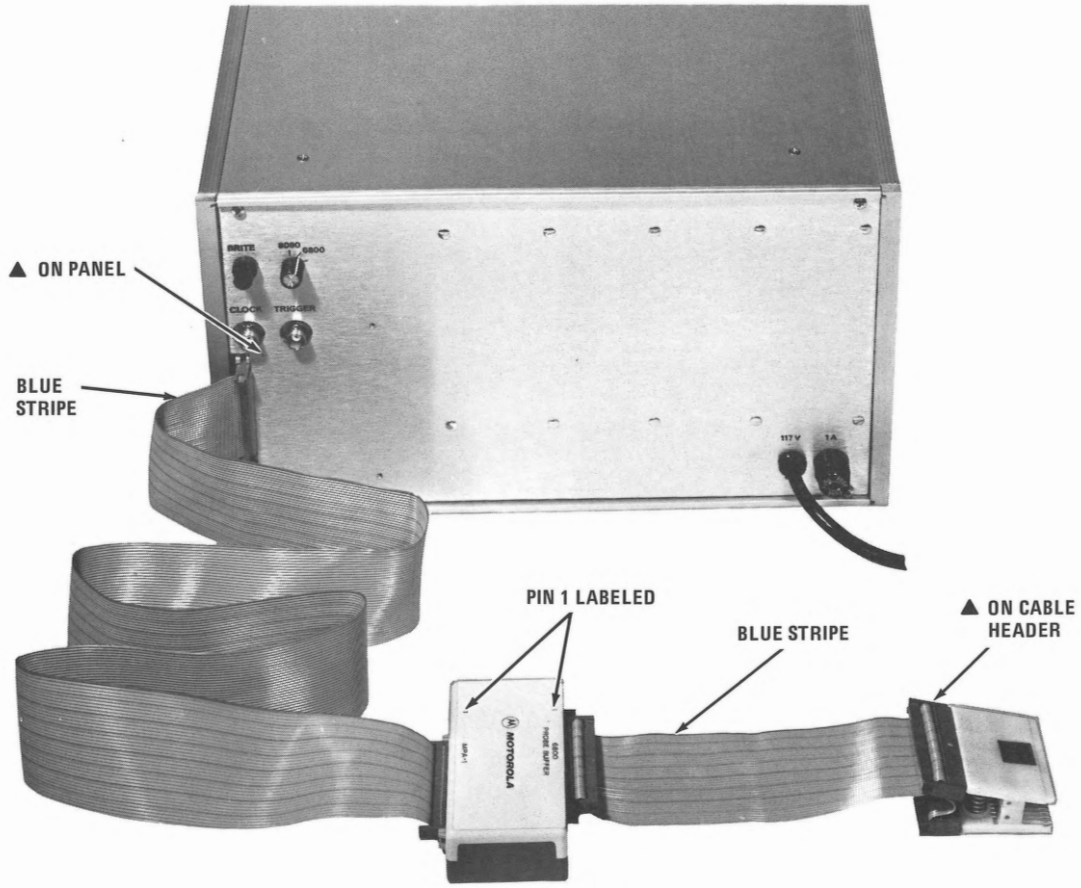


Figure 5. Connecting Probe Buffer and Test Clip

4b. If connection will be made to the Back Panel Connector of the EXORcisor, the blue marking of the 50-conductor cable should be positioned at the **REAR** of the Back Panel Connector. (See Figure 39.)

4c. If connection will be made without the prearranged feature of the Probe Buffers, refer to Table 10 for Probe Buffer pin assignments.

Some MPU sockets have raised edges that can make it difficult to obtain good connections with the IC test clip. (See Figure 6.) This difficulty can be remedied in a number of ways:

a. Remove the excess material with a cutter or file.

b. Plug the MPU into an "intermediate" socket that does not have raised edges, and plug the MPU plus socket into the circuit board.

c. Remove the socket from the circuit board and replace with a more suitable unit.

2.3 CAPTURE TIMING

The MPA–1 is set up at the factory for the capture time indicated on the tag attached to the unit. Figure 7 illustrates the Latch Clock T_n calculations and the setup for the DIP switch S7. Table 2 on the same page indicates the switch setup for different values of T_n. For example, the Motorola EXORcisor ™ would need T_n = 420 nsec, which is switch 2 of S7 in the ON position. The timing for any processor and associated memory can be calculated by the formula given.

2.4 CONTROLS, INDICATORS, AND CONNECTORS

Figure 8 gives the location of all MPA–1 controls, indicators and connectors. Each of these is functionally in Table 3.

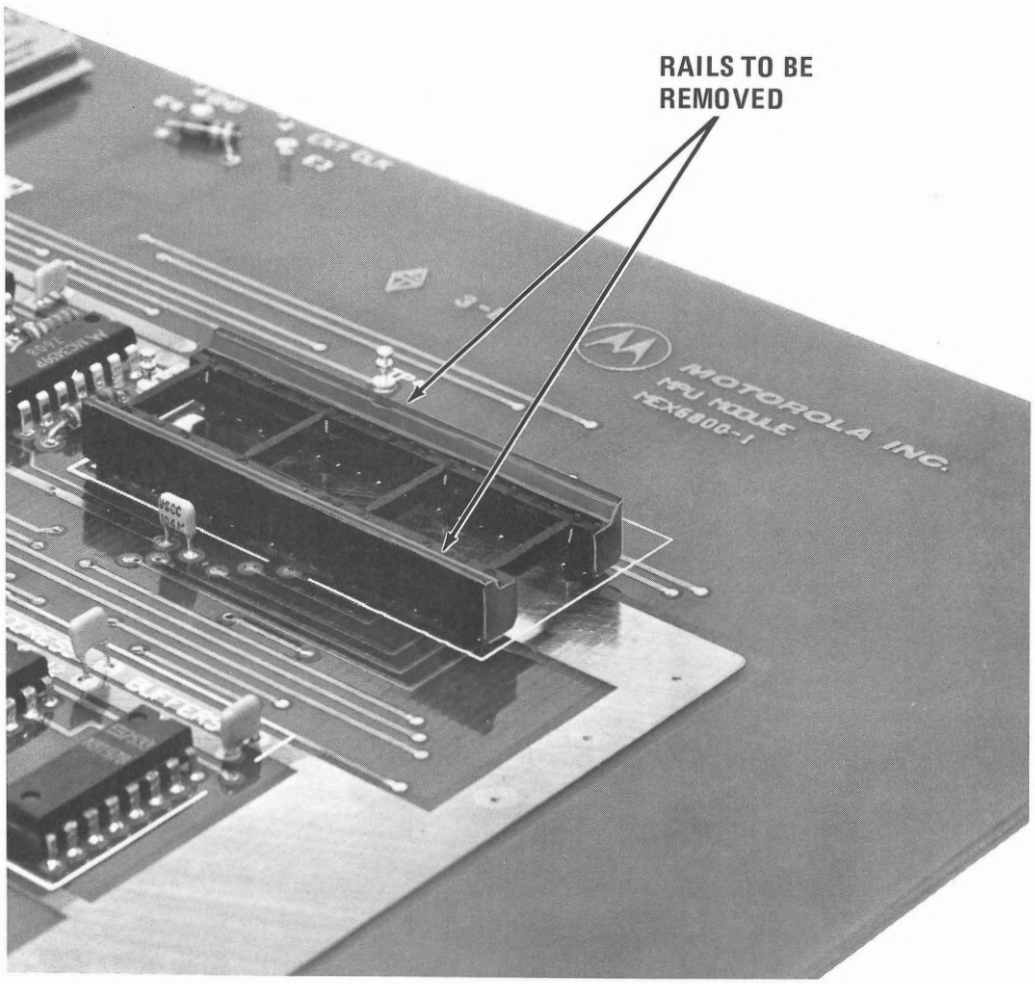
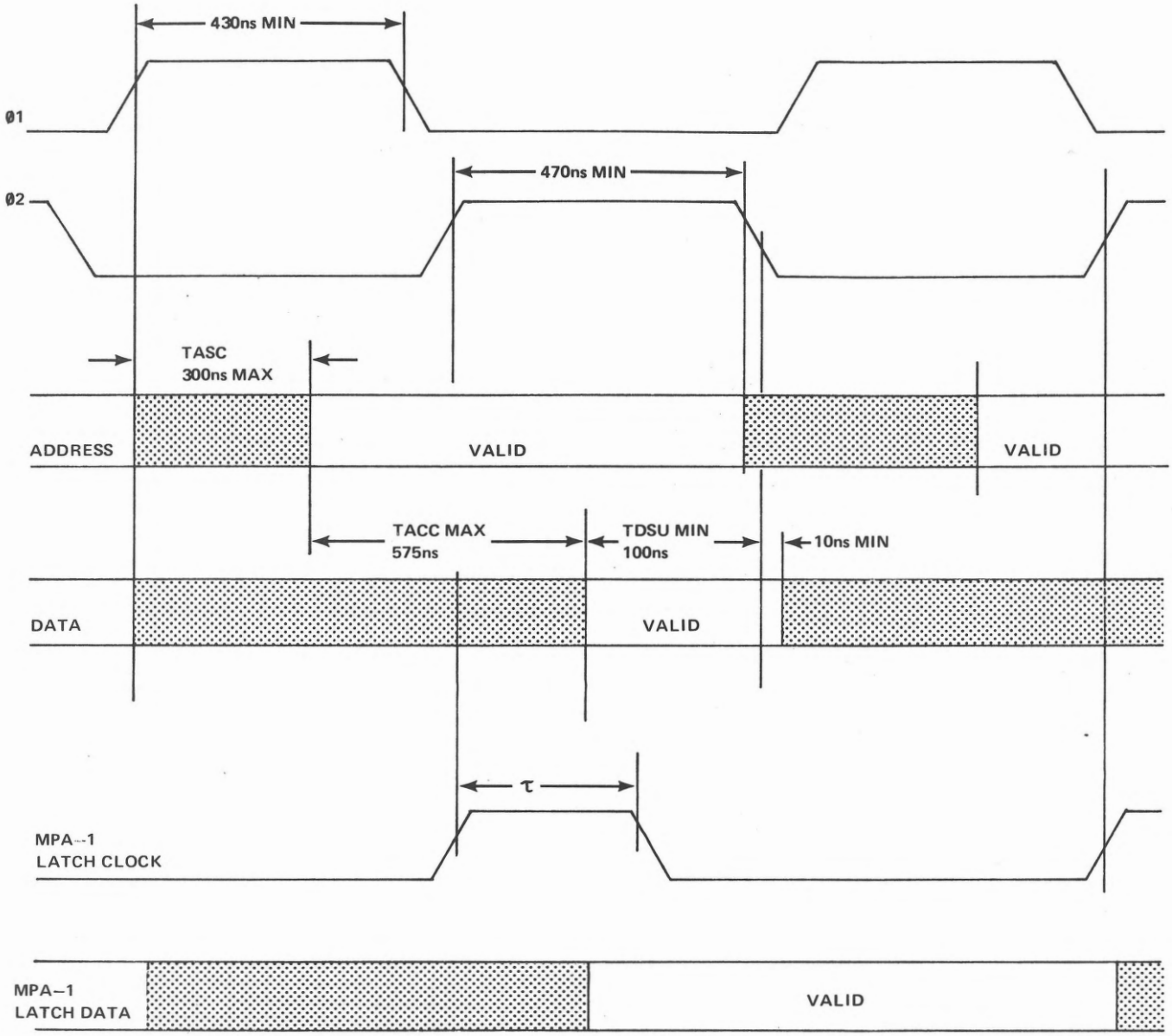


Figure 6. MPU Socket

MPA–1 LATCH CLOCK τ CALCULATIONS AND TIMING SELECTION SWITCH S7



DATA NOT VALID

DATA HAS TO BE VALID AT LEAST T_{DSU} = 100ns BEFORE END OF Ø2 (MICROPROCESSOR SPECIFICATION)

τ CAN BE CALCULATED BY USING FOLLOWING FORMULA:

$300 + T_{ACC} - Ø1 < \tau < Ø2 + 10$ (nsec), AND SET THE SWITCH S7 FROM THE ADJACENT TABLE SUCH THAT YOU CAN GET NEAREST VALUE.

EXORCISOR ™ = 420nsec

TABLE 2. CAPTURE TIMING: S7 SWITCH SETTINGS

	SWITCH S7 AT D1 LOCATION		
τn sec	S7–1	S7–2	S7–3
45			
140			X
420		X	
515		X	X
940	X		
1080	X		X
1315	X	X	
1455	X	X	X

NOTE: X INDICATES 'ON' POSITION ON SWITCH.

Figure 7. Capture Timing

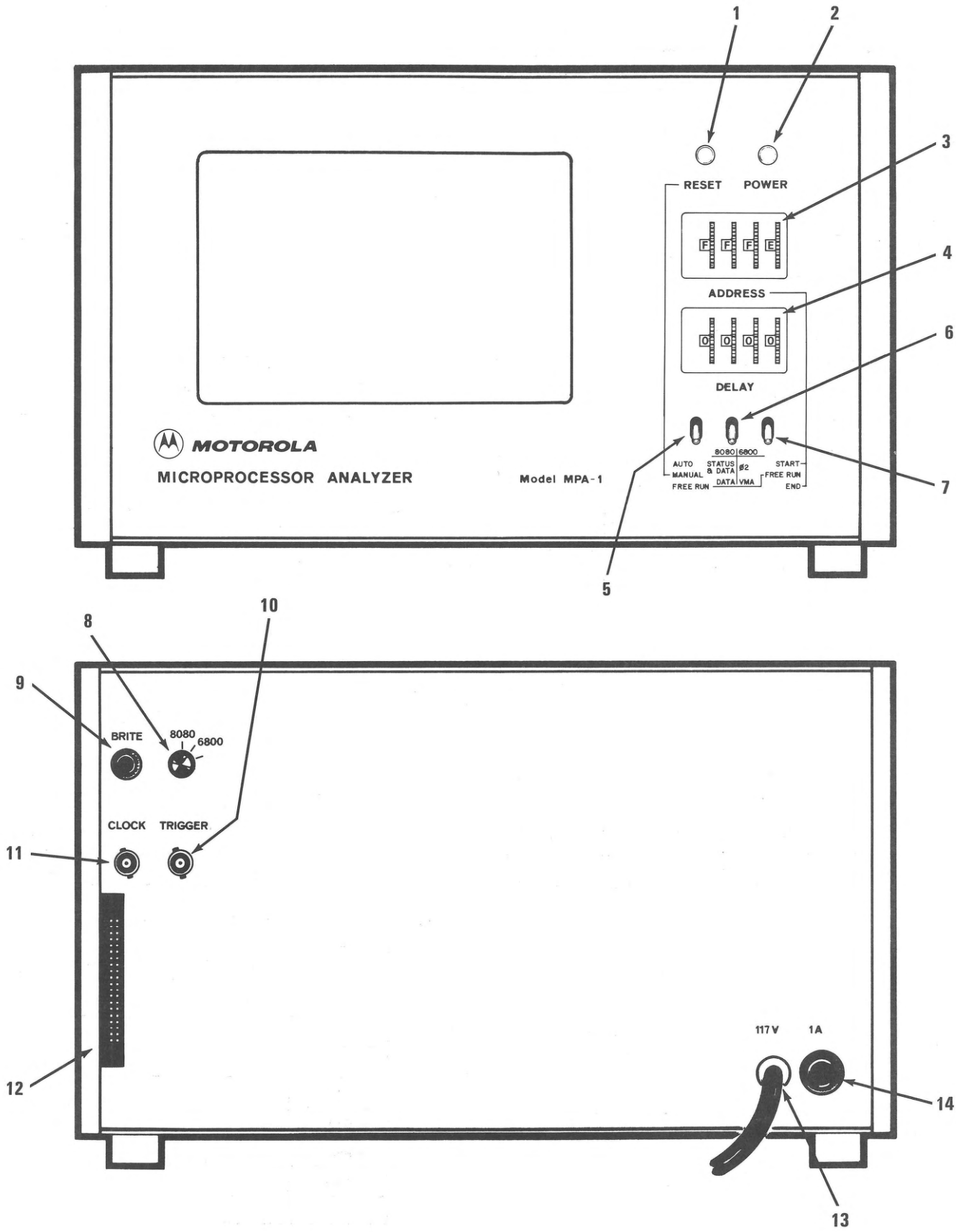


Figure 8. MPA–1 Front and Back Panel

Table 3. Controls, Indicators, and Connectors

FRONT PANEL

1. RESET. Arms trigger address recognition circuit. Lights when trigger is armed. Extinguishes when trigger word is recognized.

2. POWER. Line Power Switch. Lights when power is on.

3. ADDRESS. Thumbwheel switches for entry of trigger address in hexadecimal form.

4. DELAY. Thumbwheel switches for entry of delay in hexadecimal form.

5. AUTO/MANUAL. Selects display mode.

   a. AUTO. Automatically blanks display and rearms trigger after 250 mSec.

   b. MANUAL. When selected, pressing RESET switch blanks display and arms trigger. Display starts 31 words after trigger word is recognized and continues until RESET is pressed again.

   * c. FREE RUN. When selected, allows continuous display of processor activity. Momentary selection of FREE RUN with this switch captures a random segment of processor activity.

6. Ø2/VMA. Selects clocking signal for data capture circuitry.

   INTEL 8080.

   a. STATUS AND DATA. Status bits are captured and alternated with data.

   b. DATA. Status bits are ignored.

   MOTOROLA 6800.

   a. Ø2. A 6-character word is captured for each Ø2 clock cycle. Allows data capture in direct relationship to real time.

   b. Ø and VMA. Clocks input circuitry with logical product or Ø2 and VMA. Processor cycles for which VMA = 0 are not captured.

7. START/END. Selects trigger mode.

   a. START. When selected, trigger word becomes the first word in the display. (Delay set to 0000.)

   * b. FREE RUN. Setting for FREE RUN mode.

   c. END. When selected, trigger word becomes the last word in the display. (Delay set to 0000).

BACK PANEL

8. 8080/6800. Selects processor type.

9. BRITE. Display brightness control. (Other display controls are located on monitor board.)

10. TRIGGER. Output BNC for trigger address recognition pulse. (Negative logic).

11. CLOCK. Output BNC for clock signal. (Negative logic).

12. INPUT. Connector for address, data, and clock signals. ▲ indicates pin 1.

13. 117V. MPA–1 line cord.

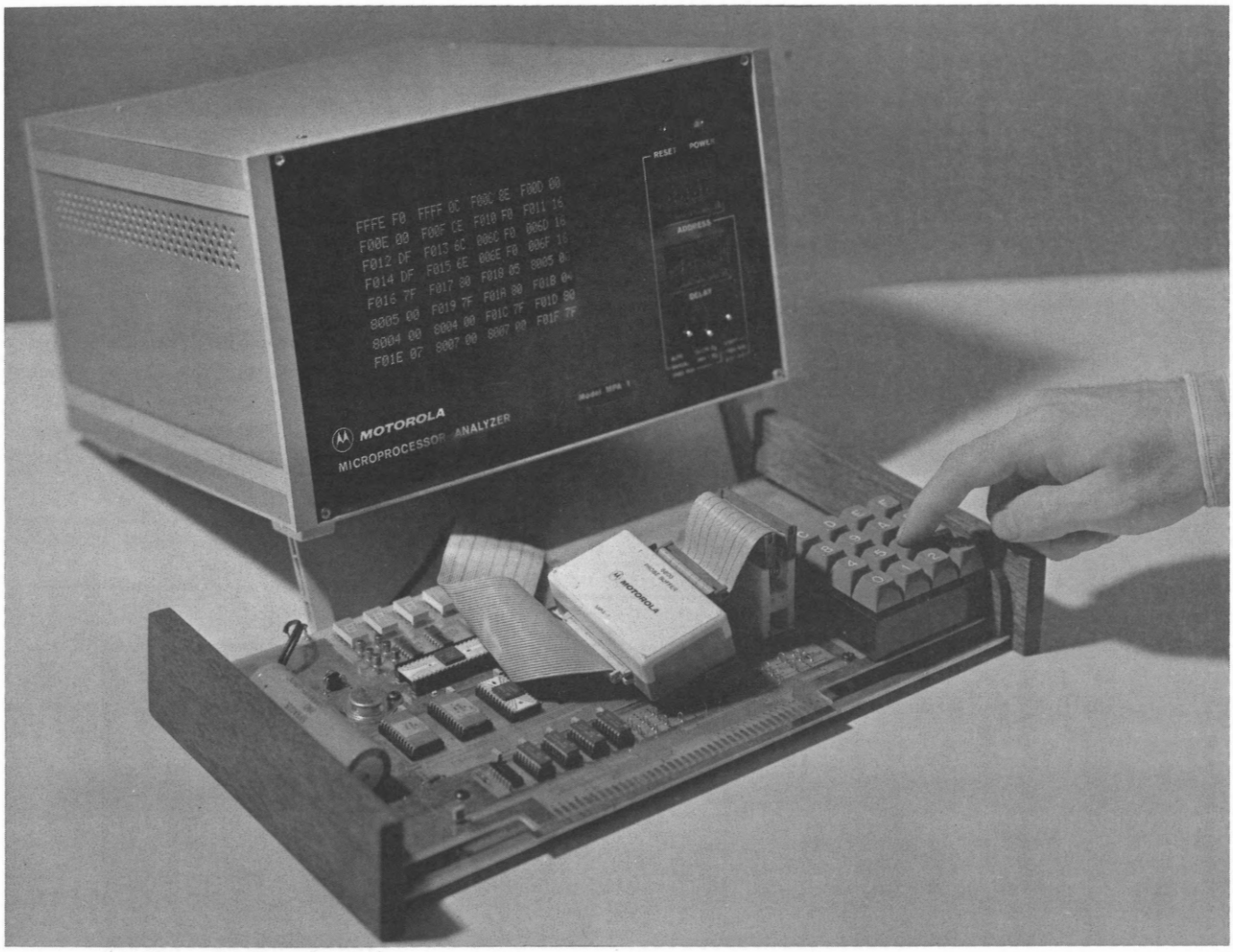
14. FUSE. 1.0–A time-delay power line fuse for 105–132V AC operation. (Use 0.5–A time-delay fuse for 220V AC operation.)

* The AUTO/MANUAL switch and the START/END switch must both be set to FREE RUN to select that mode of operation.

SECTION 3
OPERATING EXAMPLES

3.1 INTRODUCTION

This section illustrates how the MPA–1 can be used in actual applications. Examples are given for the M6800, 8080, and PPS–4. Programs and corresponding displays are presented side by side to illustrate the interrelationships. Supplementary information is supplied to aid in interpreting the displays.

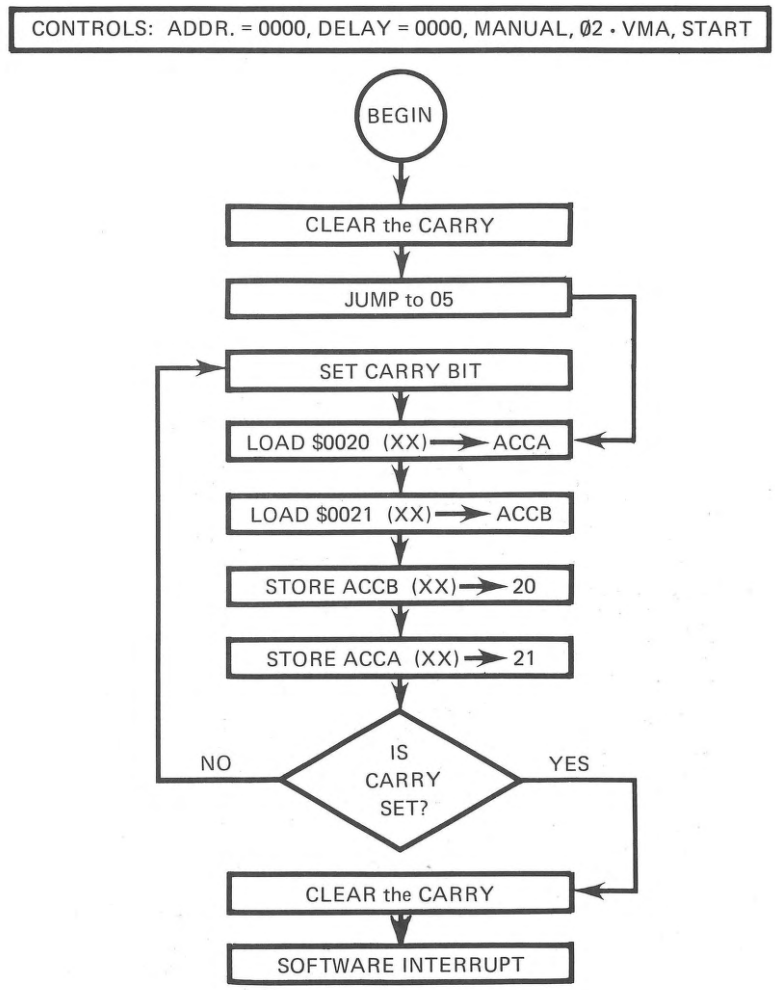


3.2 M6800 EXAMPLE PROGRAM AND DISPLAY

The program in this example exchanges the contents of RAM locations 20 and 21. By utilizing the carry bit as a flag, it makes a second pass to restore the locations to their original condition.

The program listing and flow chart are shown below. The Figure 9 shows the display of a program segment with Ø2 • VMA clocking and displays cycles only when VMA is true. Refer to Table 4, cycle-by-cycle summary of the MC6800 machine instructions. The table shows the cycles for which VMA is high.

The Section 3.3 uses the example program to illustrate other modes of operation. Section 3.4 shows Ø2 clocking using the same program.



PROGRAM

```
0000    ØC          CLC
0001    7E 00 05    JMP $05
0004    ØD          SEC
0005    96 20       LDA A $20
0007    D6 21       STA A $21
0009    D7 20       STA B $20
000B    97 21       STA A $21
000D    24 F5       BCC
000F    ØC          CLC
ØØ1Ø    3F          SWI
  .
  .
  .
ØØ2Ø    AA
ØØ21    BB
```

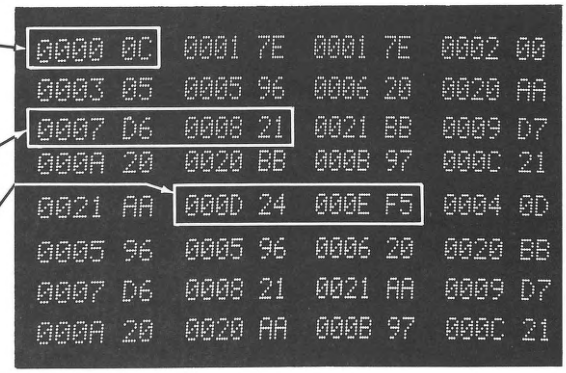


Figure 9. First 32 Words of Program Execution

3.3 M6800 EXAMPLES–DISPLAY MODES

In **START DISPLAY** mode, Figure 10, the MPA–1 captures and displays the trigger word and the following 31 words in the order of their execution. The trigger word for this display is 0000, as can be seen in the upper left corner. This mode is helpful for tracing program flow.

CONTROLS: ADDR. = 0000, DELAY = 0000
MANUAL, Ø2 • VMA, START

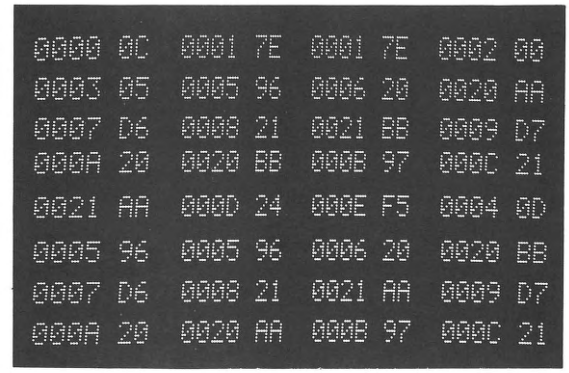


Figure 10. Start Display

In **START DELAYED** mode, the 32-word display can be delayed digitally by up to 65k clock cycles. The display in Figure 11 is delayed by 10 hex or 16 clock cycles. This mode is useful in applications where the desired data does not immediately follow the trigger word.

CONTROLS: ADDR. = 0000, DELAY = 0010
MANUAL, Ø2 • VMA, START

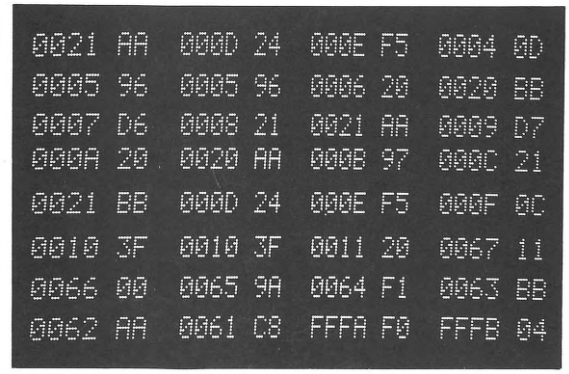


Figure 11. Start Delay

In **END DISPLAY** mode, Figure 12, the MPA–1 continuously stores program execution. When the trigger word is recognized, it displays the trigger word and the previous 31 words in a "negative time" format. The trigger word is the last word on the screen. This mode is useful in tracing backward to find hardware and software errors.

CONTROLS: ADDR. = 000F, DELAY = 0000
MANUAL, Ø2 • VMA, END

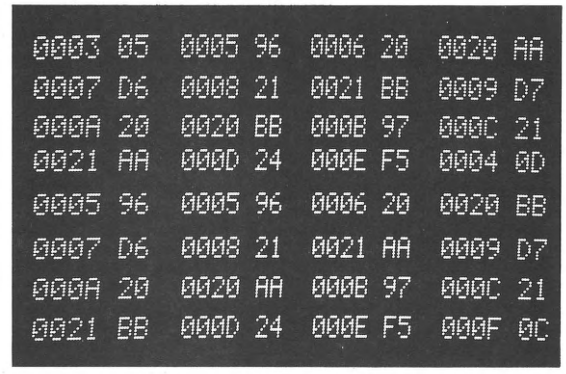


Figure 12. End Display

In **END DELAYED** mode, the word is digitally delayed and the trigger word is recognized the same as in End Display. With a delay of 16 clocks, the trigger word will be centered on the display. This is useful for examining the activity preceding and following the trigger word. Figure 13 shows this mode.

CONTROLS: ADDR. = 000F, DELAY = 0010
MANUAL, Ø2 • VMA, END

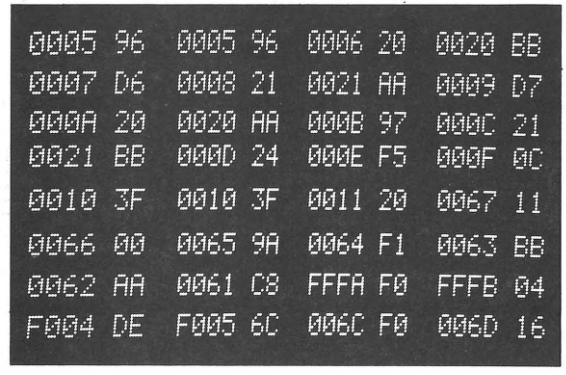


Figure 13. End Display

3.4 M6800 EXAMPLES–Ø2 CLOCKING

The displays in Figure 14 show the comparison between Ø2 • VMA and Ø2 only clock modes. In the Ø2 only mode, the MPA–1 captures data on every clock pulse, thus displaying in one-to-one relation with real time. The extra cycles highlighted on the figure are times when the VMA signal is low. Refer to Table 4, the cycle by cycle summary, for information on when VMA is low. In most cases, Ø2 • VMA mode is used because it produces a more compact display. Typical applications for the Ø2 mode are loop timing and time critical program calculations.

CONTROLS: ADDR. = 0000, DELAY = 0000, MANUAL, Ø2 , START

PROGRAM

0000	ØC	CLC
0001	7E 00 05	JMP $05
0004	ØD	SEC
0005	96 20	LDA A $20
0007	D6 21	LDA B $21
0009	D7 20	STA B $20
000B	97 21	STA A $21
000D	24 F5	BCC
000F	ØC	CLC
ØØ1Ø	3F	SWI
	.	
	.	
	.	
ØØ2Ø	AA	
ØØ21	BB	

```
0000 0C  0001 7E  0001 7E  0002 00
0003 05  0005 96  0006 20  0020 AA
0007 D6  0008 21  0021 BB  0009 D7
000A 20  0020 BB  000B 97  000C 21
0021 AA  000D 24  000E F5  0004 0D
0005 96  0005 96  0006 20  0020 BB
0007 D6  0008 21  0021 AA  0009 D7
000A 20  0020 AA  000B 97  000C 21
```

```
0000 0C  0001 7E  0001 7E  0002 00
0003 05  0005 96  0006 20  0020 AA
0007 D6  0008 21  0021 BB  0009 D7
000A 20  0020 20  0020 BB  000B 97
000C 21  0021 21  0021 AA  000D 24
000E F5  000F F5  0004 F5  0004 0D
0005 96  0005 96  0006 20  0020 BB
0007 D6  0008 21  0021 AA  0009 D7
```

Figure 14. Comparison of Ø2 · VMA and Ø2 Clocking

3.5 M6800 EXAMPLE–FREE RUN

The program segment used in this example illustrates the use of the **FREE RUN** mode in finding program hang-ups or software faults. In Figure 15, the address 003 is fixed in each word of the display and all other characters are blurred. The fixed numbers indicate little or no activity on those address lines. Evidently, the program hang-up is in the vicinity of address 0030. Figure 16 shows **FREE RUN** stopped using the **START/END** switch. By placing the switch in **START** or **END**, the MPA–1 will display the last 32 addresses and data captured by the instrument. From this section of code a trigger address can be determined and **END DISPLAY** triggering can be used to work backward to the source of the error. The program hang-up can be located on the software listing and the fault corrected.

CONTROLS: ADDR. = 0030, DELAY = 0000, FREE RUN, Ø2 • VMA, FREE RUN

PROGRAM

```
.
.
.
0030          4F          CLR   A
0031          4C          INC   A
0032          1B          ABA
0033          49          ROL   A
0034    7E    00    30    JMP   $30
.
.
.
```

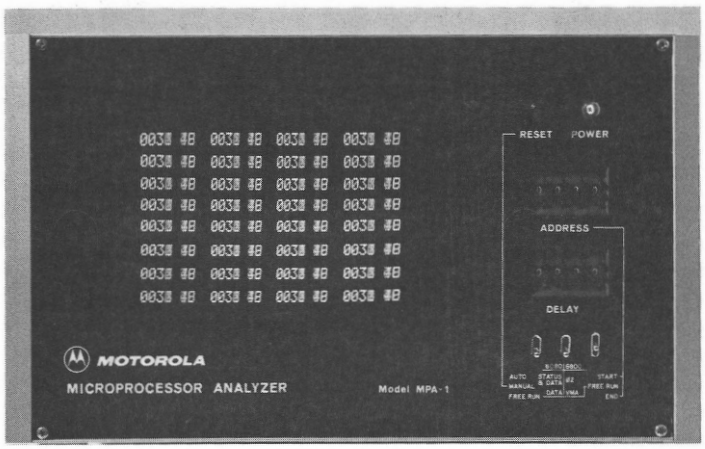


Figure 15. Free Run

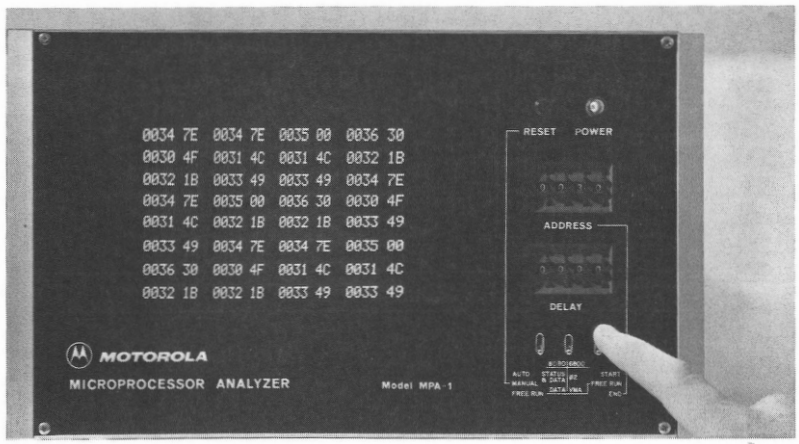


Figure 16. Free Run Stopped

3.6 M6800 SAMPLE PROGRAM – DOUBLE OP CODES

The execution of a 1-byte, 2-cycle, inherent instruction causes the following instruction to be fetched twice. The first OP code is the 2nd cycle of the inherent instruction. The second Op code is the actual instruction fetch. Double Op codes are illustrated in the following example (See Figure 17). They occur after the CLRA and the ROLA instructions.

CONTROLS: ADDR. = 0000, DELAY = 0000, MANUAL, Ø2 VMA, START

PROGRAM

```
0000    4F          CLR   A
0001    96  20      LDA   A   $20
0003    49          ROL   A
0004    97  21      STA   A   $21
0006    3F          SWI
  .
  .
  .
0020    01
0021    XX
```

```
0000 4F  0001 96  0001 96  0002 20
0020 01  0003 49  0004 97  0004 97
0005 21  0021 02  0006 3F  0007 D6
0067 07  0066 00  0065 9A  0064 F1
0063 02  0062 AA  0061 C0  FFFA F0
FFFB 04  F004 DE  F005 6C  006C F0
006D 16  F006 6E  F007 00  F016 7F
F017 80  F018 05  8005 04  8005 00
```

Figure 17. Double Op Code Fetches

3.7 M6800 SAMPLE PROGRAM AND DISPLAY – SUBROUTINE CALL

The program in this example calls the subroutine SWAP to exchange the data in RAM locations 20 and 21. The jump to subroutine (JSR) instruction causes the MPU to save the return address in RAM locations indexed by the stack pointer (SP), and jump to the starting address of the subroutine. When the return instruction (RTS) is encountered, the return address program counter low and high (PCL and PCH) are removed from the stack and program execution resumes at that location.

The display in Figure 18 shows the address being saved on the stack. This illustrates the use of the MPA–1 in tracing subroutine calls and stack operations. When the program returns to **MAIN**, a software interrupt (SWI) is encountered causing the return address and machine registers with status to be saved in the stack. Figure 19 shows the saving of machine status.

CONTROLS: ADDR. = 0000, DELAY = 0000, MANUAL, Ø2 • VMA, START

PROGRAM

```
                          *MAIN
0000    BD  00  10        JSR     SWAP
0003    3F                SWI


                          *SUBROUTINE SWAP
0010    96  20    SWAP    LDA  A  $20
0012    D6  21            LDA  B  $21
0014    D7  20            STA  B  $20
0016    97  21            STA  A  $21
0018    39                RTS


0020    AA
0021    BB
```

```
0000 BD  0001 00  0002 10  0010 96
0067 03  0066 00  0002 10  0010 96
0011 20  0020 AA  0012 D6  0013 21
0021 BB  0014 D7  0015 20  0020 BB
0016 97  0017 21  0021 AA  0018 39
0019 80  0066 00  0067 03  0003 3F
0004 97  0067 04  0066 00  0065 9A
0064 F1  0063 AA  0062 BB  0061 C8
```

Figure 18. Subroutine Call–Stack Operations

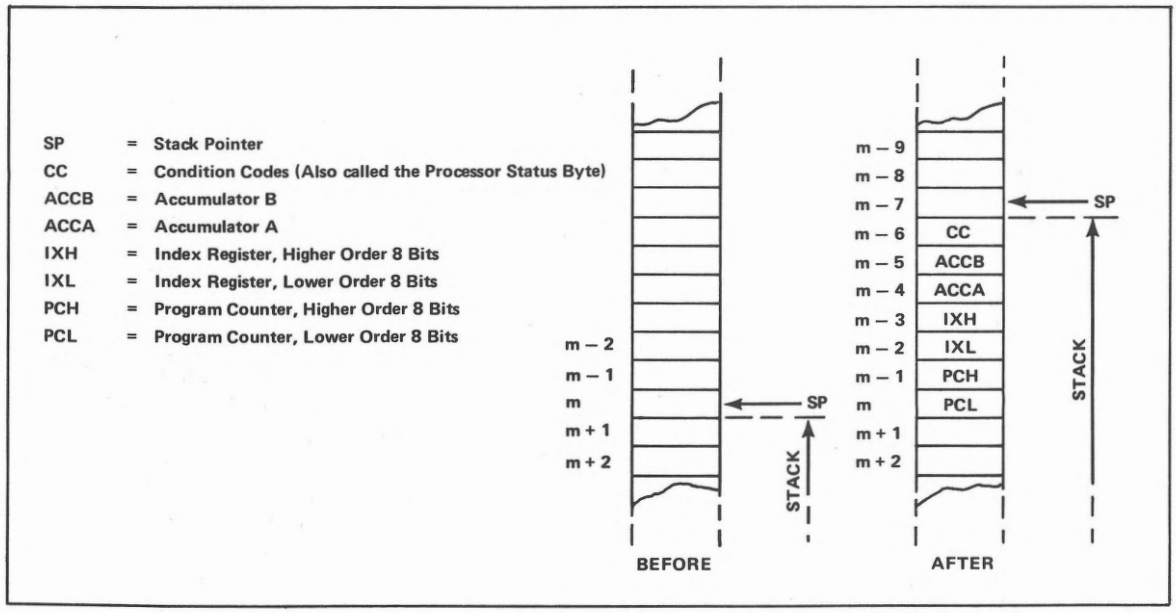


Figure 19. Saving the Status of the Microprocessor in the Stack

TABLE 4. SUMMARY OF CYCLE BY CYCLE OPERATION

Table 4 provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to Addressing Mode and Number of Cycles per instruction. (In general, instructions with the same Addressing Mode and Number of Cycles execute in the same manner; exceptions are indicated in the table.)

TABLE 4 – OPERATION SUMMARY

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data
CPX LDS LDX	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data (High Order Byte)
		3	1	Op Code Address + 2	1	Operand Data (Low Order Byte)
DIRECT						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data
CPX LDS LDX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data (High Order Byte)
		4	1	Operand Address + 1	1	Operand Data (Low Order Byte)
STA	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address
		3	0	Destination Address	1	Irrelevant Data (Note 1)
		4	1	Destination Address	0	Data from Accumulator
STS STX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	0	Address of Operand	1	Irrelevant Data (Note 1)
		4	1	Address of Operand	0	Register Data (High Order Byte)
		5	1	Address of Operand + 1	0	Register Data (Low Order Byte)
INDEXED						
JMP	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data
CPX LDS LDX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data (High Order Byte)
		6	1	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)

TABLE 4 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INDEXED (Continued)						
STA	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Current Operand Data
		6	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		7	1/0 (Note 3)	Index Register Plus Offset	0	New Operand Data (Note 3)
STS STX	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data (High Order Byte)
		7	1	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
JSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Index Register	1	Irrelevant Data (Note 1)
		8	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
EXTENDED						
JMP	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	1	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data
CPX LDS LDX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data (High Order Byte)
		5	1	Address of Operand + 1	1	Operand Data (Low Order Byte)
STA A STA B	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	1	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	0	Operand Destination Address	1	Irrelevant Data (Note 1)
		5	1	Operand Destination Address	0	Data from Accumulator
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Current Operand Data
		5	0	Address of Operand	1	Irrelevant Data (Note 1)
		6	1/0 (Note 3)	Address of Operand	0	New Operand Data (Note 3)

TABLE 4 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
EXTENDED (Continued)						
STS STX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	0	Address of Operand	1	Irrelevant Data (Note 1)
		5	1	Address of Operand	0	Operand Data (High Order Byte)
		6	1	Address of Operand + 1	0	Operand Data (Low Order Byte)
JSR	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	1	Subroutine Starting Address	1	Op Code of Next Instruction
		5	1	Stack Pointer	0	Return Address (Low Order Byte)
		6	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		7	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		8	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		9	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
INHERENT						
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
DES DEX INS INX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Previous Register Contents	1	Irrelevant Data (Note 1)
		4	0	New Register Contents	1	Irrelevant Data (Note 1)
PSH	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Accumulator Data
		4	0	Stack Pointer – 1	1	Accumulator Data
PUL	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Operand Data from Stack
TSX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	0	New Index Register	1	Irrelevant Data (Note 1)
TXS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Index Register	1	Irrelevant Data
		4	0	New Stack Pointer	1	Irrelevant Data
RTS	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Address of Next Instruction (High Order Byte)
		5	1	Stack Pointer + 2	1	Address of Next Instruction (Low Order Byte)

TABLE 4 – OPERATION SUMMARY (Concluded)

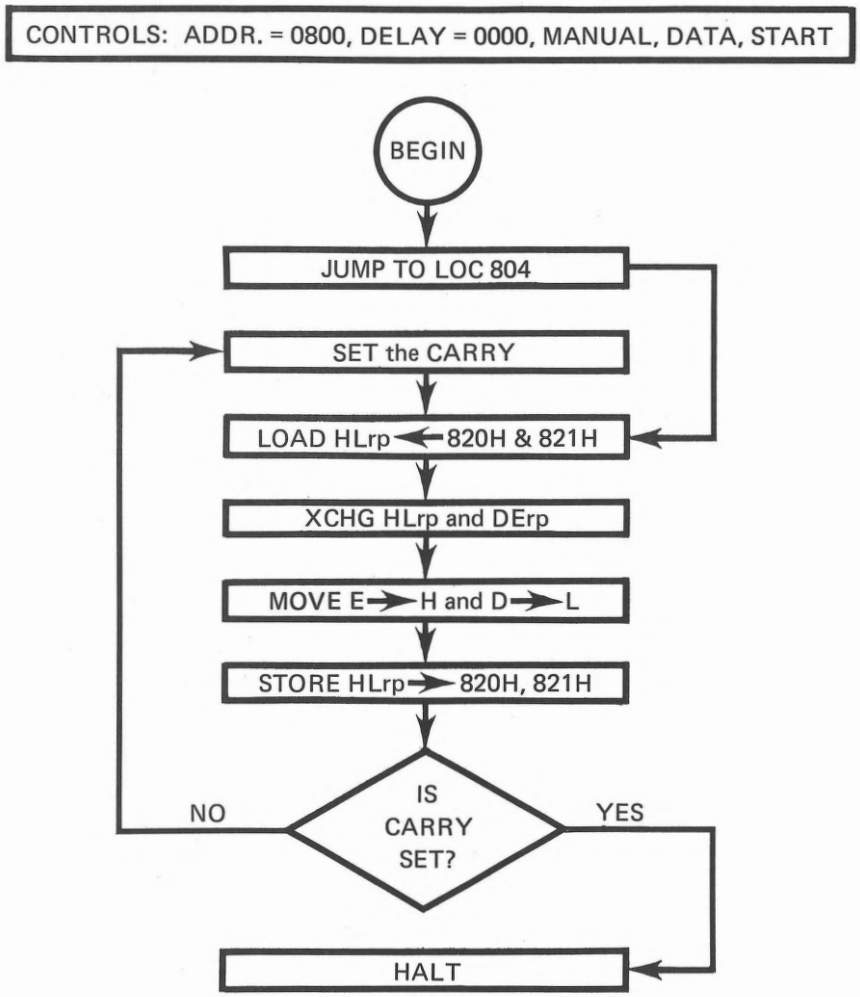
Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INHERENT (Continued)						
WAI	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6 (Note 4)	1	Contents of Cond. Code Register
RTI	10	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Contents of Cond. Code Register from Stack
		5	1	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	1	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	1	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	1	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	1	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	1	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 1)
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6	0	Contents of Cond. Code Register
		10	0	Stack Pointer – 7	1	Irrelevant Data (Note 1)
		11	1	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	1	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE						
BCC BHI BNE BCS BLE BPL BEQ BLS BRA BGE BLT BVC BGT BMI BVS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		4	0	Branch Address	1	Irrelevant Data (Note 1)
BSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		8	0	Subroutine Address	1	Irrelevant Data (Note 1)

Note 1. If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.
Note 2. Data is ignored by the MPU.
Note 3. For TST, VMA = 0 and Operand data does not change.
Note 4. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low; Address Bus, R/W, and Data Bus are all in the high impedance state.

3.8 INTEL 8080 SAMPLE PROGRAM AND DISPLAY

The program in this example parallels the Motorola M6800 example in Section 3.2. The flow chart and program listing are shown with the MPA–1 display. Figure 20 shows the display resulting from the execution of the program.

The program exchanges the contents of RAM locations 20H and 21H. It utilizes the carry bit as a flag and makes a second pass to restore the locations to their original condition.



PROGRAM

0800	C3	04	08	JMP	804H
0803	37			STC	
0804	2A	20	08	LHLD	820H
0807	EB			XCHG	
0808	63			MOV	H,E
0809	6A			MOV	L,D
080A	22	20	08	SHLD	820H
080D	D2	03	08	JNC	803H
0810	76			HLT	
0820	AA				
0821	BB				

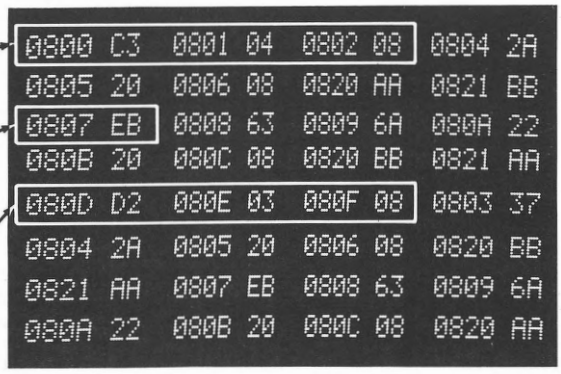


Figure 20. First 32 Words of Program Execution

3.9 INTEL 8080 SAMPLE PROGRAM AND DISPLAY – SUBROUTINE CALL

The program in this example calls the subroutine SWAP to exchange data in RAM locations 20H and 21H. This illustrates the use of the MPA–1 in viewing stack operations and tracing subroutines. When the program encounters the CALL instruction, the return address is saved on the stack and execution continues at the first line of the subroutine. When the RETURN (RET) instruction is encountered, the return address is popped off the stack and execution continues at 1+ the address it left fron. These operations are pointed out on the display in Figure 21 below.

CONTROLS: ADDR. = 0800, DELAY = 0000, MANUAL, DATA, START

PROGRAM

```
                                    ; MAIN PROGRAM
0800    31  30  08                  LXI   SP, 830H
0803    CD  07  08                  CALL  SWAP
0806    76                          HLT


                                    ; SUBROUTINE SWAP
08071   2A  20  08  SWAP            LHLD  820H
080A    EB                          XCHG
080B    63                          MOV   H,E
080C    6A                          MOV   L,D
080D    22  20  08                  SHLD  820H
0810    C9                          RET


0820    AA
0821    BB
```

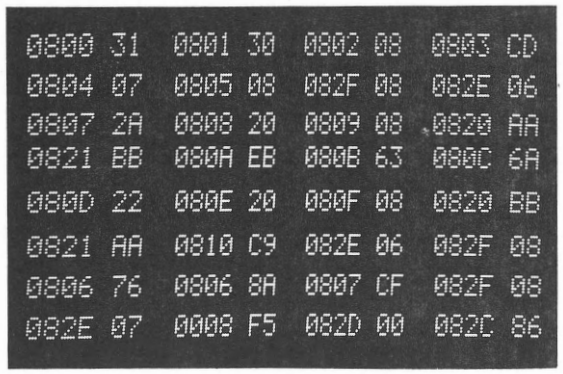


Figure 21. Subroutine Call

3.10 INTEL 8080 SAMPLE PROGRAM AND DISPLAY – STATUS AND DATA

The program in this example illustrates the capability of the MPA–1 to display STATUS information for 8080 type processors. STATUS information is sent out by the processor during SYNC time, at the beginning of each machine cycle. The status appears first on the MPA–1 display followed by the data. Both have the same address since they pertain to only one instruction. The Figure 22 shows the display of the program and status. Refer also to Table 5, status table for 8080.

CONTROLS: ADDR. = 0800, DELAY = 0000, MANUAL, STATUS & DATA, START

PROGRAM

0800	77			MOV	M,A
0801	78			MOV	A,B
0802	DB	00		IN	0
0804	D3	00		OUT	0
0806	C5			PUSH	B
0807	C1			POP	B
0808	C3	00	08	JMP	0800H

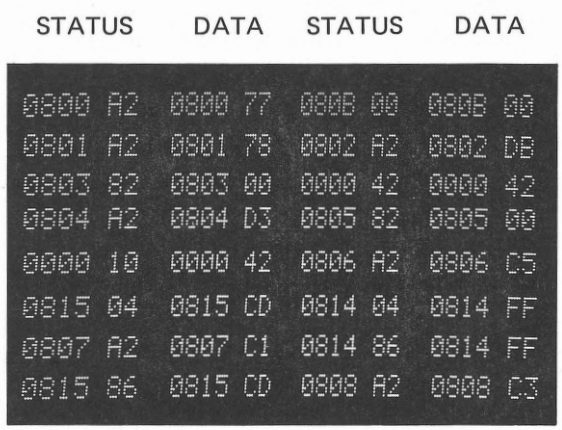


Figure 22. Status/Data Display

Table 5. Intel Status Bytes

STATUS	MPA–1 DISPLAY	INTA D_0	WO D_1	STACK D_2	HLTA D_3	OUT D_4	M1 D_5	INP D_6	MEMR D_7
INSTRUCTION FETCH	A2	0	1	0	0	0	1	0	1
MEMORY READ	82	0	1	0	0	0	0	0	1
MEMORY WRITE	00	0	0	0	0	0	0	0	0
STACK READ	86	0	1	1	0	0	0	0	1
STACK WRITE	04	0	0	1	0	0	0	0	0
INPUT READ	42	0	1	0	0	0	0	1	0
OUTPUT WRITE	10	0	0	0	0	1	0	0	0
INTR ACKNOWLEDGE	23	1	1	0	0	0	1	0	0
HALT ACKNOWLEDGE	8A	0	1	0	1	0	0	0	1
INTR ACKNOWLEDGE WHILE HALT	29	1	0	0	1	0	1	0	0

3.11 ROCKWELL PPS–4 SAMPLE PROGRAM AND DISPLAY

The program used in this example is executed from PROM. Figure 23 shows the MPA–1 display of a segment of the execution.

The program uses the Accumulator (AC) to load the BL, BM, and BU address registers with FF. It then enters a loop that writes data to memory and decrements the address. When the AC becomes FF the transfer (T) in location ØØØC is executed and the program branches to ØØØØ.

CONTROLS: ADDR. = 0000, DELAY = 0000, MANUAL, Ø2, START

PROGRAM

0000	81	T
0001	7F	LDI
0002	19	XABL
0003	7F	LDI
0004	1B	LXA
0005	10	LBMX
0006	7F	LDI
0007	04	LBUA
0008	70	LDI
0009	3F	EX
000A	1F	DECB
000B	88	T
000C	80	T

```
0000 81  0001 7F  0002 19  0003 7F
0004 1B  0005 10  0006 7F  0007 04
0008 70  0009 3F  000A 1F  000B 88
000C 80  0000 81  0001 7F  0002 19
0003 7F  0004 1B  0005 10  0006 7F
0007 04  0008 70  0009 3F  000A 1F
000B 88  000C 80  0000 81  0001 7F
0002 19  0003 7F  0004 1B  0005 10
```

Figure 23. Execution in PROM

3.12 ROCKWELL PPS–4 SAMPLE PROGRAM AND DISPLAY

The program used in this example is similar to the previous example. The display, Figure 24, shows the program activity in RAM as a result of the execution of the program listed below.

CONTROLS: ADDR. = A000, DELAY = 0000 , MANUAL, 02, START

PROGRAM

0000	81	T
0001	7F	LDI
0002	19	XABL
0003	7F	LDI
0004	1B	LXA
0005	10	LBMX
0006	7F	LDI
0007	04	LBUA
0008	70	LDI
0009	3F	EX
000A	1F	DECB
000B	88	T
000C	11	LABL
000D	3F	EX
000E	1F	DECB
000F	8C	T
0010	8C	T

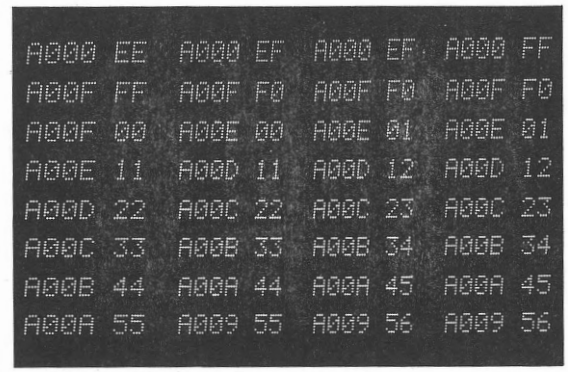


Figure 24. Program Activity in RAM

SECTION 4
FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This section provides a functional description of the MPA–1. The principles of operation are discussed in terms of the Motorola M6800 microprocessor. Once operation with the M6800 is understood, application to other processors is straightforward. The description is divided into seven subsections for ease of comprehension. Each subsection refers to the relevant block diagrams and schematics which are located in Section 6. Used in conjunction with the Troubleshooting Chart, the Functional Description can be a helpful service aid.

4.2 DATA CAPTURE MODE

The MPA–1 is connected to the processor under test by means of an external Probe Buffer. The Probe Buffer uses MC14049 CMOS Hex Inverter/Buffers and short lead lengths to minimize loading of the processor busses. Buffered MPU signals enter the MPA–1 through the 40-pin back panel connector. After entering the MPA–1, all MPU signals pass through 7486 Quad 2-Input Exclusive OR Gates which can selectively invert logic levels under control of DIP Switch S4. (See Figure 40 for the Data Capture Block Diagrams, and Figure 44 for the Logic Board Schematic.) Address and data bits can be inverted in groups of 4; Ø2 and VMA can be inverted individually. Address and data bits are then separated from the clock and VMA signals and latched by 7475 4-Bit Latches under control of an adjustable delay pulse derived from the MPU Ø2 clock or Ø2•VMA. The clocking mode is selected by the front panel switch S3. The DIP switch S7 is used to set the delay T_n to allow for different memory speeds and processor types. (See Table 2 and Figure 7 for details of S7 switch settings.)

The address in the latches is compared with the address in the thumbwheel switches by 7486 Exclusive OR Gates. When the trigger address is recognized, the recognition latch is set. This latch, composed of cross-coupled NAND Gates, enables Ø2 or Ø2 • VMA to pulse the delay down counter. The delay counter is composed of four 74193 4-Bit Up/Down Counters which are preset from the **DELAY** thumbwheel switches on the front panel. The delay must be satisfied before data capture can begin. When the down counter reaches zero, it enables the display mode (**START** or **END**), selected by the front panel switches. If **START** mode is selected, **CAPTURE COMPLETE** is delayed by 31 clock cycles so that the trigger word and the following 31 cycles of processor activity can be loaded into the 2518 Hex 32-Bit Shift Register. If **END** mode is selected, the Shift Register is updated during each MPU clock cycle. Recognition of the trigger word terminates capture and sends **CAPTURE COMPLETE** to the display circuitry.

4.3 DATA DISPLAY MODE

CAPTURE COMPLETE indicates that the data in the Shift Register (S.R.) is ready to be read out. During read out, the S.R. is controlled by the MPA–1 internal clock rather than the clock of the MPU under test. To initialize the display, the start of S.R. recirculation must be synchronized with the start of a monitor refresh cycle. The coincidence of **CAPTURE COMPLETE** and **TOP-OF-SCREEN (T.O.S.)** sets **DISPLAY ENABLE** which in turn starts the display. (See Figure 41 for the Display Mode Block Diagram and Figure 44 for the Logic Board Schematic.)

The source of the MPA–1 clock is a Motorola 6.912 MHz crystal with an integral TTL buffer. The crystal frequency is initially divided by 4 to produce DOT, a 579 nSec signal used to intensify the 7 dots on the wiggle display. (See Figure 25.)

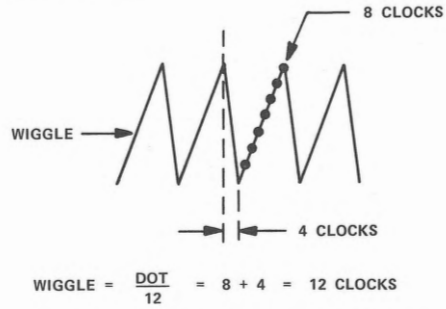


Figure 25. Wiggle Scan of a Column

The signal **DOT** is then divided by 12 to produce **WIGGLE**, a 150 kHz signal used to form the characters of the wiggle scan display. **WIGGLE** is divided by 6 to produce **CHAR.**, which is the character width counter. Each character on the wiggle scan is 5 columns wide and one additional column for the space between characters (See Figure 26), accounting for 6 wiggle periods.

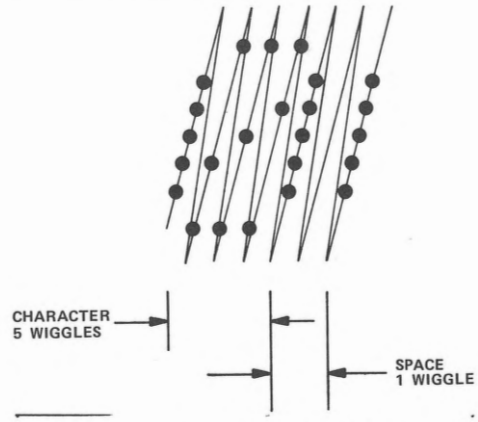


Figure 26. Wiggle Scan of a Character

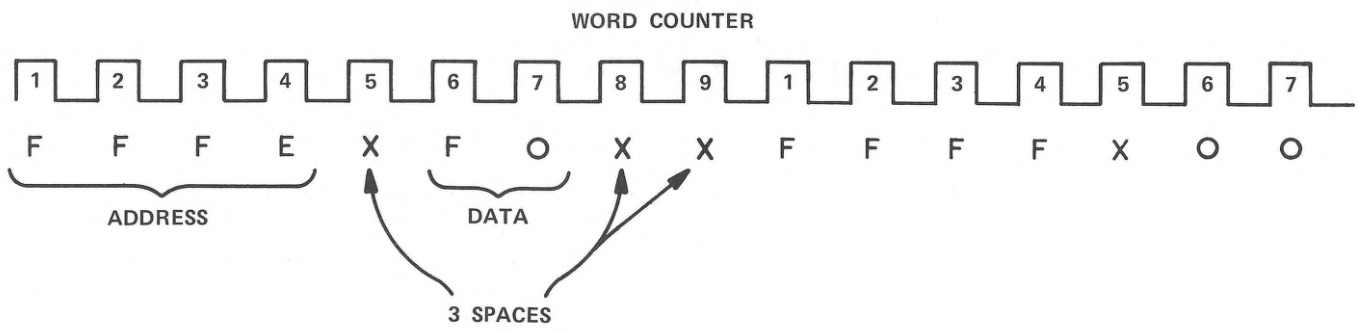


Figure 27. Word Format

The output of the character counter is used to clock the **WORD** counter, which determines the length of the words on the screen. This counter is controlled by an auxiliary counter that determines if the **WORD** counter will divide by 9 or 14. Each word, consisting of four digits of address and two of data, is 9 characters in length, including 3 spaces. (See Figure 27.)

The counter must divide by 14 at the end of the line so that 5 extra character times can be included for retrace time to the next line. Horizontal sync is also derived from this counter. The output of the **WORD** counter clocks the **ROW** counter to produce line positioning information. The outputs from this counter (V_1, V_2, and V_3) drive a 3-bit D to A converter, located on the Monitor Board.

The output of the **WORD** counter (4 bits) is decoded into select signals by the **WORD DECODER**, a 7442 BCD to Decimal Decoder. The output of the **WORD DECODER** is used to select individual characters from the DM8097 **TRI-STATE BUFFERS.** Six lines enable the DM8097 outputs and 4 bits of hexadecimal information are sampled and converted to ASCII by a 74188A ROM. The hex digits address the ROM and ASCII information is presented at the outputs as data. The 3257 5 x 7-Bit Character Generator requires ASCII input to produce dot matrix characters. The output of the **CHARACTER GENERATOR** is in a column scanned dot matrix format. This is multiplexed by a 74151 8-Line to 1-Line Data Selector to produce serial information. The **WIGGLE** counter furnishes a 3-bit address to the multiplexer so that the dot information is synchronous with **WIGGLE.** This information is clocked by the 579 nSec **DOT** pulse to produce video output.

4.4 FREE RUN

The **FREE RUN** mode is a combination of **DATA CAPTURE** and **DATA DISPLAY** modes. The front panel switch S2 (AUTO/MANUAL) is set to the **FREE RUN** position, forcing the **TRIGGER** line to be true (ground). The MPA–1 ignores the address comparator and a continuous address recognized condition exists. The front panel switch S1 (**START/END**) is also set to the **FREE RUN** position, forcing **CAPTURE COMPLETE** to be true. With these switch settings, the MPA–1 will alternately capture and display contiguous segments of MPU activity.

The data and address information are clocked into the 7475 4-Bit Latches and transferred to the S.R. at the MPU clock rate. When the display circuitry senses T.O.S., the S.R. receives a recirculate input, causing the data capture to momentarily stop and the S.R. to recirculate the 32 words it contains at that time. When a refresh cycle is completed, the recirculate signal drops and data is captured until T.O.S. is recognized again.

4.5 MONITOR

The display monitor used in MPA–1 is a wiggle scanned CRT. Horizontal sync, vertical positioning, video information, and the wiggle inputs originate on the logic board. (Refer to Figures 42 and 45 for the MONITOR BLOCK DIAGRAM and SCHEMATIC.) The monitor operates on ±12 volts DC supplied by the power supply module.

The horizontal input to the monitor board provides synchronization between the **WORD** counter and the **FREE RUNNING OSCILLATOR.** When the last word on a given line has been displayed, the monitor must retrace and be ready to display the next line. Transistors Q11 and Q12 make up the oscillator, and Q13, the **HORIZONTAL DEFLECTION AMPLIFIER,** drives the horizontal coils of the deflection yoke.

The **WIGGLE** input, a 150 kHz signal, is amplified by Q1, Q2, and Q3 to increase the amplitude to 11 volts peak-to-peak. **WIGGLE** is then combined with a staircase to produce a sawtooth scanning pattern on the CRT screen. The intensified dots that make up the characters are on the rising edge of the sawtooth pattern. (See Figure 25.)

The **VERTICAL** inputs (V1, V2, and V3) are digital information for positioning the rows of the display. The transistors Q6, Q7, and Q8 combine the digital information into a 16.6 mSec staircase output. The signal is amplified and combined with **WIGGLE** to create the 150 kHz wiggle pattern, scanning at 62.5 Hz. The transistors Q9, Q10, and Q17, Q18 make up the **VERTICAL DEFLECTION AMP-**

LIFIER which drives the vertical coils of the deflection yoke.

The **VIDEO** input consisting of serialized dot information is applied to a common base amplifier Q14, and sent to the cathode of the CRT to modulate the beam.

High voltage for the 9" CRT is developed by transformer T1 and a solid-state **HIGH VOLTAGE MULTIPLIER.** The high voltage is set at the factory and should not be readjusted. The brightness of the display is adjusted by varying the voltage applied to the control grid of the CRT. The **BRIGHTNESS** potentiometer, R50, is located on the back panel of the MPA–1. The range of the brightness is controlled by the **BRIGHTNESS LIMITER,** R51, which is located on the Monitor Board.

4.6 POWER SUPPLY

The MPA–1's power supply provides regulated output voltages of +12 volts, –12 volts, and +5 volts DC. (Refer to Figure 46, the schematic diagram for the power supply.) The supplies for all three voltages are zener diode regulated and adjustable. (Refer to Figure 33 for adjustment locations.) R_3, R_{13}, and R_7 are the adjustments for the +12, –12 and 5 volt supplies, respectively. Both 12 volt supplies have 1.6 amp slow blow fuses located on the circuit board. The 5 volt has a crowbar circuit for overvoltage protection. SCR1 and diode D8 make up the crowbar. When the voltage at the output rises above 5.6 volts, the SCR fires and shorts the output of the supply. This feature prevents damage to the integrated circuits on the logic board. The +5 volt supply has a 2 amp fast blow fuse. Refer to the schematic (Figure 48) for conversion to 230V operation.

4.7 PROBE BUFFERS

Probe Buffers are the media used to sample data from the MPU which is being tested. Motorola MC14049 CMOS Hex Inverter/Buffers are used to buffer all processor signals into the MPA–1. Probe Buffers are completely passive elements with respect to the circuit under test and do not provide any control functions. The use of wire wrap connections within the Probe Buffers allows the input signals to be reassigned as desired. If reinversion of the signals is necessary, switch S4 on the Logic Board can be set to produce the correct logic sense. Figure 37 shows the Probe Buffer with cover removed. The schematic diagram is shown in Figure 47.

SECTION 5.
MAINTENANCE

5.1 INTRODUCTION

This section provides the maintenance and troubleshooting information for the MPA–1 Microprocessor Analyzer. Disassembly, adjustments, and factory repair information are also given. The schematics, labeled photos, and Troubleshooting Chart are located in Section 6 at the rear of the manual. The Troubleshooting Chart (Figure 43) provides a step-by-step procedure for diagnosis of instrument failures. The labeled photos show locations of adjustments and major components. In Section 5.4, test points are given in tabular form for each major assembly. The test points are also referenced by the Troubleshooting Chart.

5.2 DISASSEMBLY

The MPA–1 cover is secured by four screws. To open the unit, remove these screws and slide the cover towards the back of the unit. The cover slides in grooves on the side support brackets of the unit.

The Logic Board and Monitor Board can be pulled up to a service position. Figure 31 shows the Logic Board in the service position. This is done by pushing the retaining clip towards the front of the cabinet and pulling the board straight up. A cutout on the boards allows the retaining clip to secure the module in the service position.

The power supply board plugs into a card edge connector on the power supply sub-assembly. It can be removed by pulling the board straight up. The power supply subassembly (Figure 28), is also removable.

The entire monitor sub-assembly (Figure 29) can be taken out by removing four screws in the bottom plate.

5.3 ADJUSTMENTS

MONITOR

The display monitor has positioning controls located on the monitor PCB. See labeled photo, Figure 32 for the location of these components. The following list explains the operation of each control:

a. Vertical Centering R68 moves display up and down. Adjust for even "dark" area on top and bottom of screen.

b. Vertical Size R11 changes size of characters. Adjust for display of 8 rows of uniform size characters.

c. Horizontal Size R27 changes the width of the display. Adjust for 4 complete rows of information easily seen from the front view.

d. Horizontal Linearity R44 changes the horizontal spacing of the words. Adjust for uniform spacing.

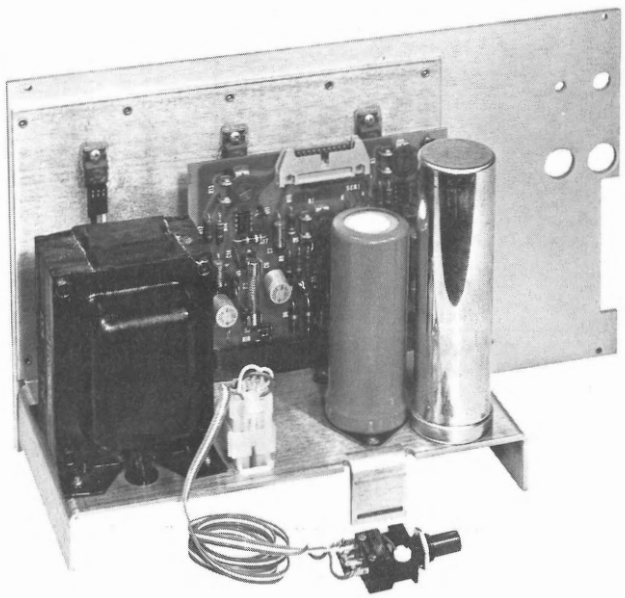


Figure 28. Power Supply Subassembly

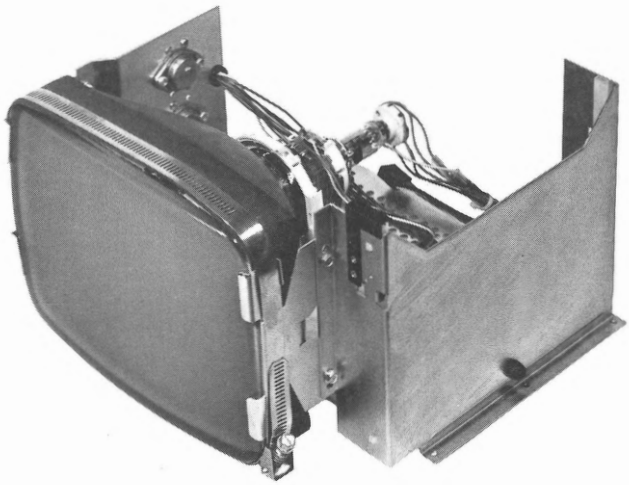


Figure 29. Monitor Subassembly

POWER SUPPLY

The power supply has controls for setting the voltage outputs of the supply. The test points are identified by Table 8 in Section 5.4 of the manual. Reference Figure 36 for the location of the components on the power supply PCB. The following list describes the controls:

a. +12 Volts R3 controls +12 volt supply. Meter test point and set for +12.0 ±0.1 volts.

b. –12 Volts R13 controls 12 volt supply. Meter test point and set for –12.0 ±0.1 volts.

c. +5 Volts R7 controls +5 volt supply. Meter the test point and set for +5.0 ±0.1 volts.

5.4 TROUBLESHOOTING CHART

The Troubleshooting Chart, Figure 43 is used for diagnostic purposes when experiencing trouble with the MPA–1. The referenced test points are located in this section. Together with the schematic diagrams and labeled photos, the source of any problems can readily be found.

The fundamentals of successful troubleshooting are a thorough understanding of the instrument's operation and correct use of the controls. Occasionally suspected malfunctions are caused by improper switch or control settings. Before attempting to troubleshoot this instrument, refer to Section 2 (Operation of Controls) and Section 4 (Functional Description).

5.5 INQUIRIES AND FACTORY REPAIR

Any questions regarding this manual or operation of the MPA–1 can be directed to:

Motorola Data Products
455 E. North Avenue
Carol Stream, Illinois 60187
TEL: (312) 690–1400
TWX: 910–252–4404

Use the model number and serial number on the tab located on the back of the unit for all inquiries.

The MPA–1 may be returned to the factory for repair in fulfillment of the warranty. When returning the unit, use the original shipping carton and packing material or similar materials to prevent damage during shipment. If the unit is sent prepaid, it will be returned prepaid. Please affix an identification tag stating the name and address of the person to whom the unit should be returned and a brief description of the difficulty encountered. For units not under warranty (1 year), a standard repair charge will be made.

Table 6. Logic Board – Test Points

Ground Reference X2–35, 37, 39

SIGNAL	TEST POINT (IC NO.–PIN NO.)	PULSE DURATION (HIGH)	PERIOD
DOT	N4–5	0.289 uSec	0.578 uSec
WIGGLE	L4–10	2.4 uSec	7.23 uSec
CHAR.	L4–15	2.2 uSec	42.0 uSec
WORD	L5–12	42.0 uSec	427.0 uSec
HORIZ.	M2–15	580.0 uSec	2.2 mSec
VIDEO (Note 1)	O3–6	0.7 mSec	2.2 mSec
T.O.S.	O2–8	16.6 mSec	16.6 mSec
V1	N1–9	2.08 mSec	4.16 mSec
V2	N1–8	4.16 mSec	8.33 mSec
V3	N1–11	8.33 mSec	16.66 mSec
TRIGGER (Note 2)	E4–12	19.0 mSec	19.0 mSec

Refer to Figure 44, Schematic for the Logic Board.

Note 1. Signal is present only in the display mode.

Note 2. Signal is continuously present only when the unit triggers on a TRIGGER WORD in the AUTO reset mode.

Table 7. Monitor – Test Points

Ground reference J4–9, 10, 11

SIGNAL	TEST POINT (COMPONENT–POINT)	LEVEL	DURATION
WIGGLE	D1 – cathode	3.5V p-p	6.9 uSec
WIGGLE/VERT.	Q5 – collector	18V p-p	16.6 mSec
VERT.	Q5 – base	9V p-p	16.6 mSec
HORIZ.	D4 – cathode	3.4V p-p	2 mSec
HORIZ. OSC.	D13 – anode	10V p-p	2 mSec
V1	D7 – anode	3.5V p-p	4.15 mSec
V2	D8 – anode	3.5V p-p	8.3 mSec
V3	D9 – anode	3.5V p-p	16.6 mSec
VIDEO *	Q14 – collector	40V p-p	2 mSec
+12V	C30 – +side	+12V D.C.	––
–12V	C5 – –side	–12V D.C.	––

Refer to Figure 45, schematic for the monitor.

* Present only in display mode.

Table 8. Power Supply – Test Points

Ground reference P4–12, 14, 15, 16, 17, 18, 19

SIGNAL	TEST POINT (COMPONENT–POINT)	LEVEL
+12V	C3 – +side	+12 volts
–12V	C10 – –side	–12 volts
+5V	D8 – cathode	+5 volts
+UNREG	C1A – +side	+18.1 volts
–UNREG	C9 – +side	+5.6 volts
UNREG5	C1B – +side	+8 volts
+UNREGFB	IC1 – 6	13.3 volts
–UNREGFB	IC3 – 6	1.6 volts
UNREG5FB	IC2 – 6	6.8 volts

Refer to Figure 46, schematic for power supply module.

SECTION 6
DIAGRAMS

6.1 INTRODUCTION

This section contains the component location photos, block diagrams, troubleshooting chart, and schematics for the Model MPA–1. The diagrams have figure numbers and are referenced by the text.

On some diagrams, DC voltages have been indicated. Appropriate test equipment only, such as a high impedance DVM or oscilloscope, should be used to measure these points. Waveforms have also been included on the monitor schematic for purposes of troubleshooting. Again, use only a high impedance oscilloscope to monitor these points.

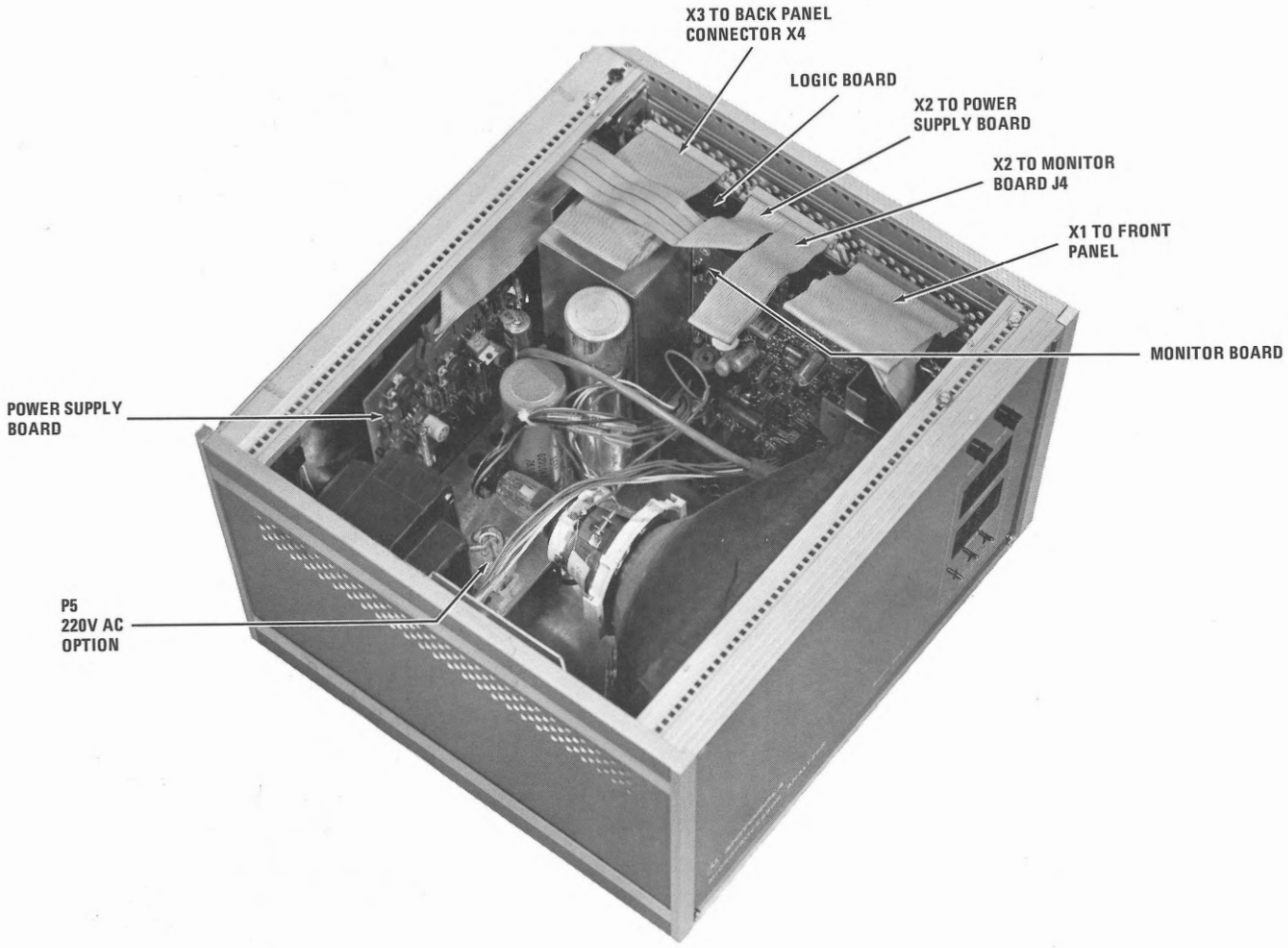


Figure 30. MPA–1 Top View

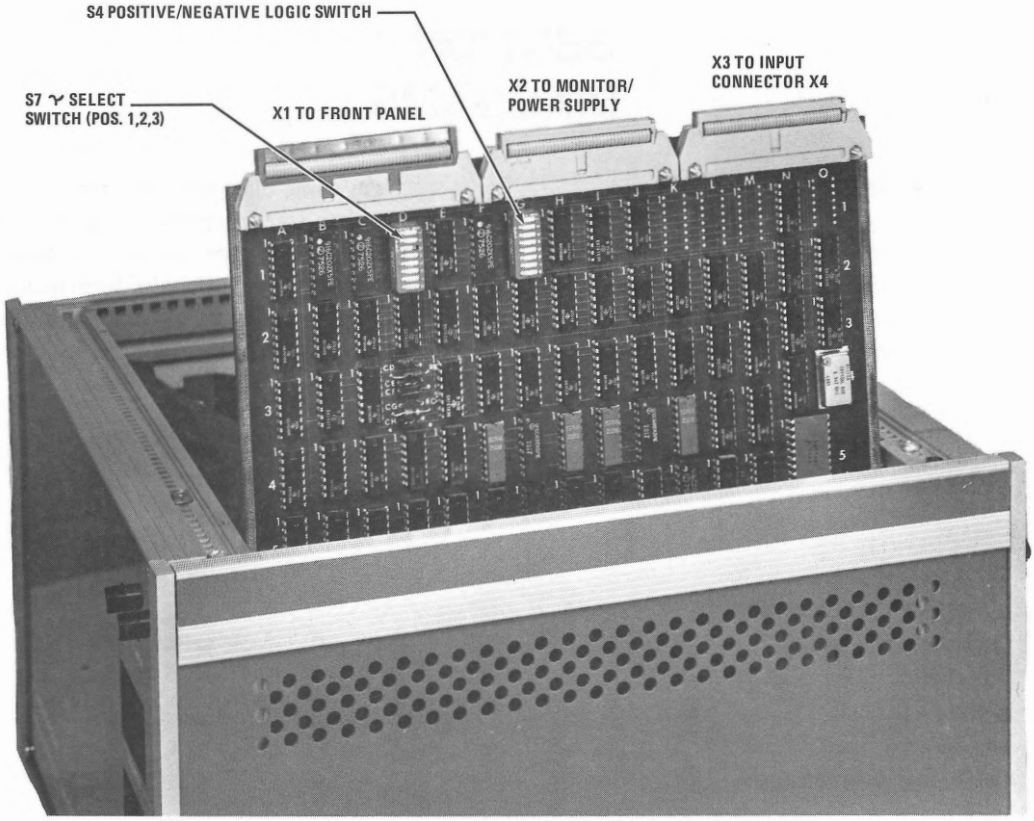

S4 POSITIVE/NEGATIVE LOGIC SWITCH
S7 ⏦ SELECT SWITCH (POS. 1,2,3)
X1 TO FRONT PANEL
X2 TO MONITOR/ POWER SUPPLY
X3 TO INPUT CONNECTOR X4

Figure 31. Logic Board Service Position

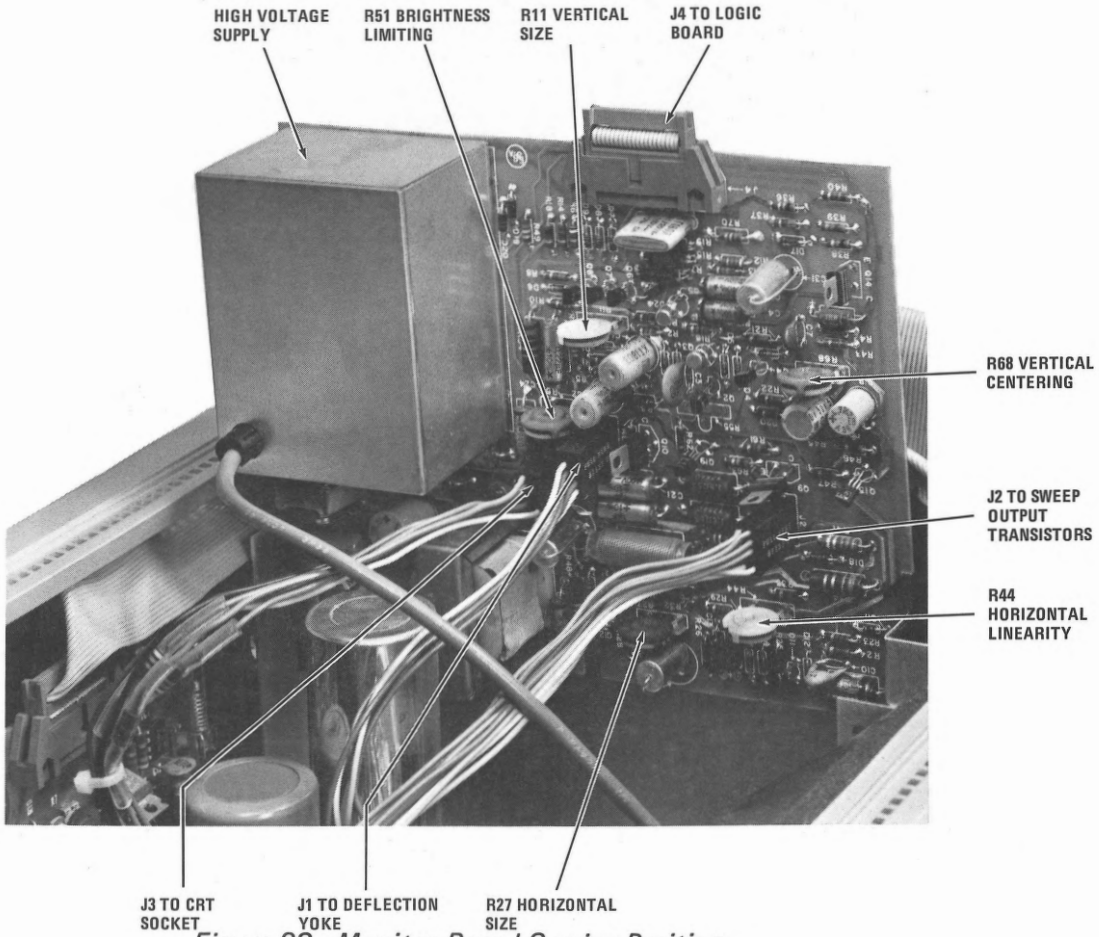


Figure 32. Monitor Board Service Position

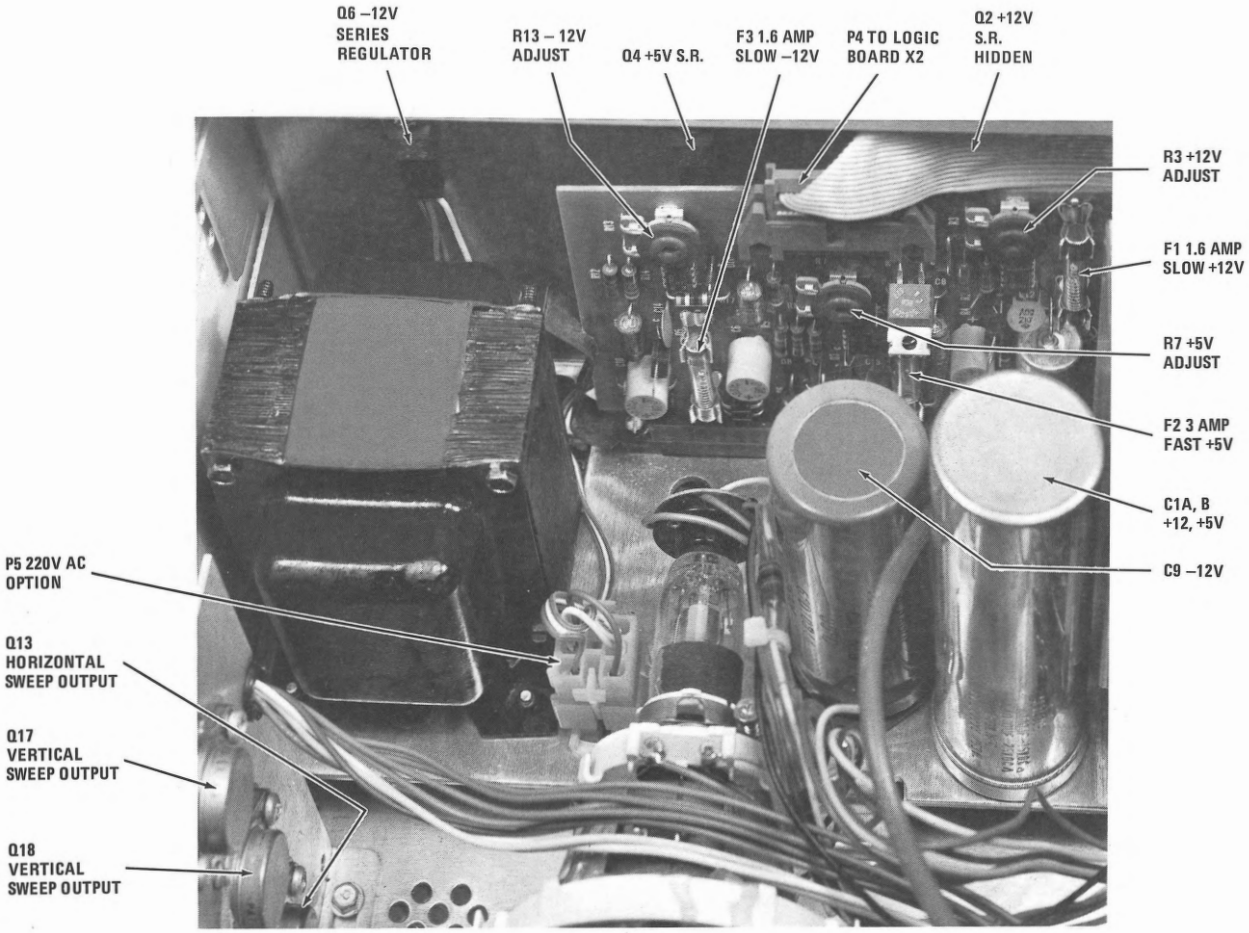


Figure 33. Power Supply Board Service Position

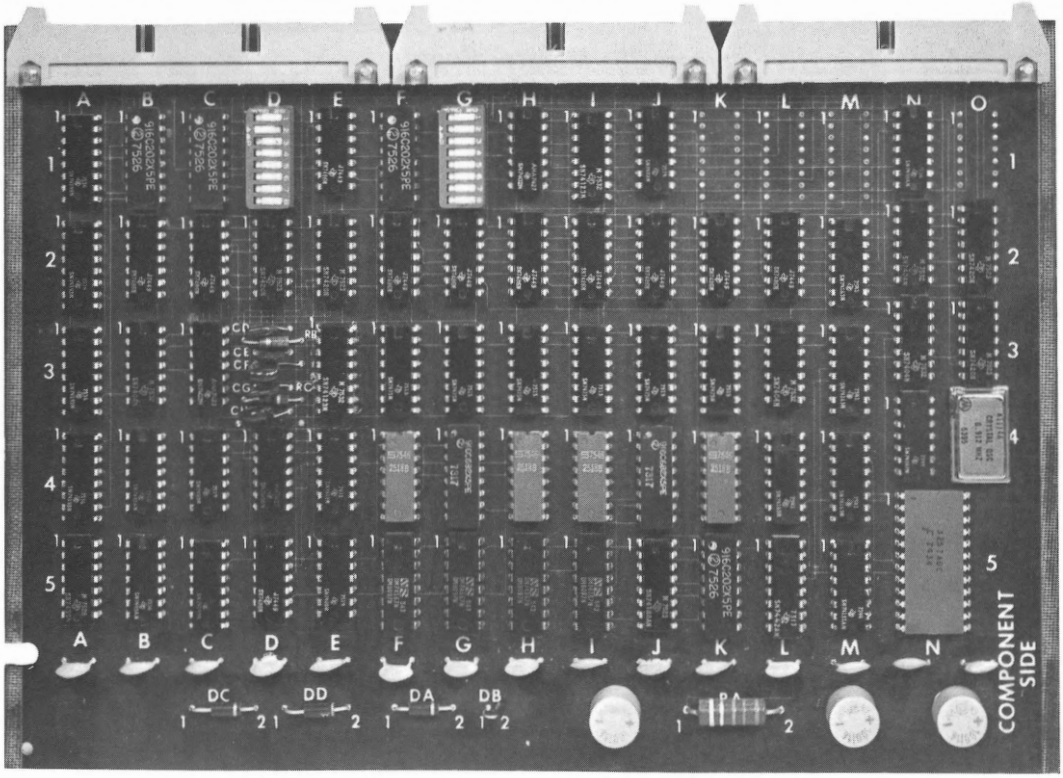


Figure 34. Logic Board

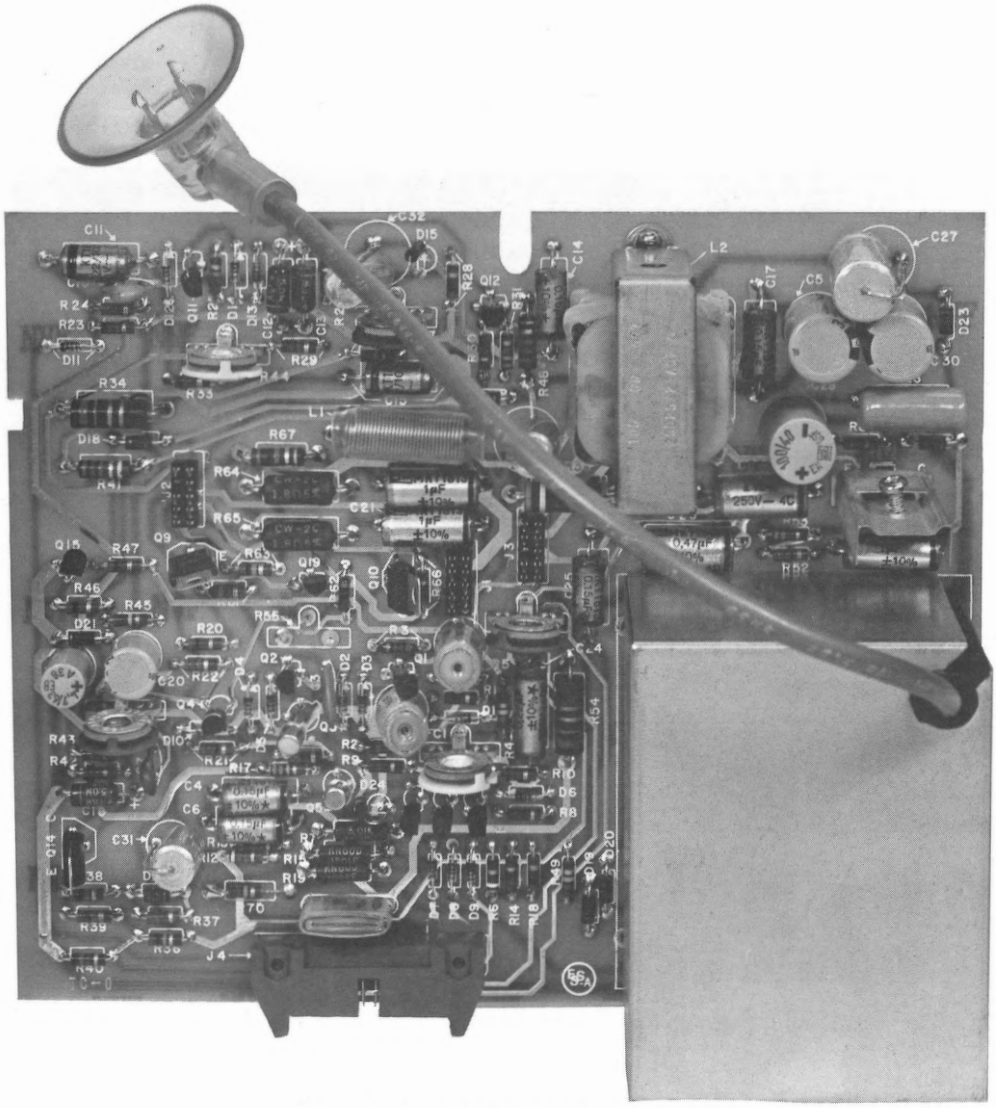


Figure 35. Monitor Board

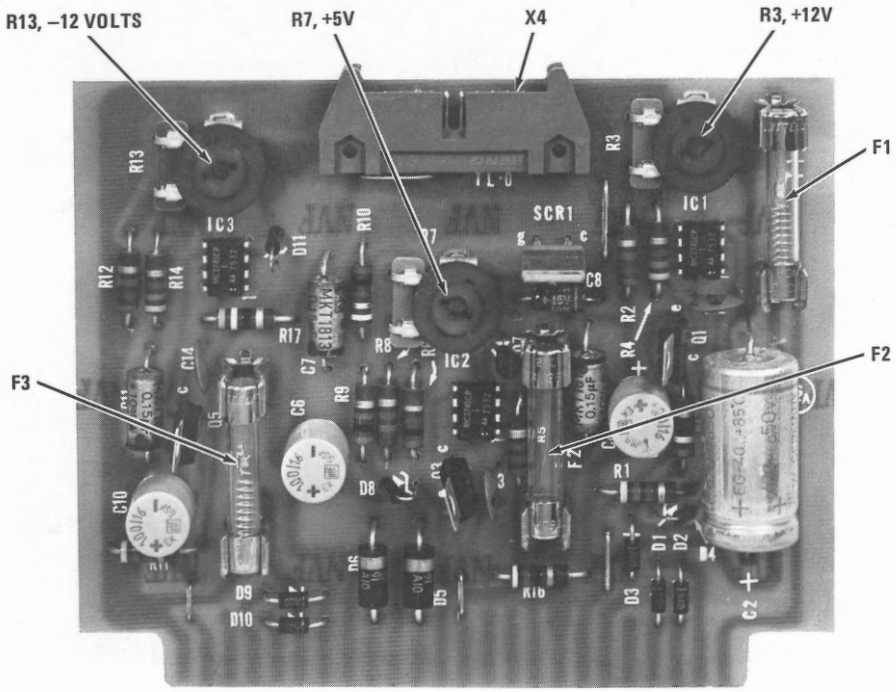


Figure 36. Power Supply Board

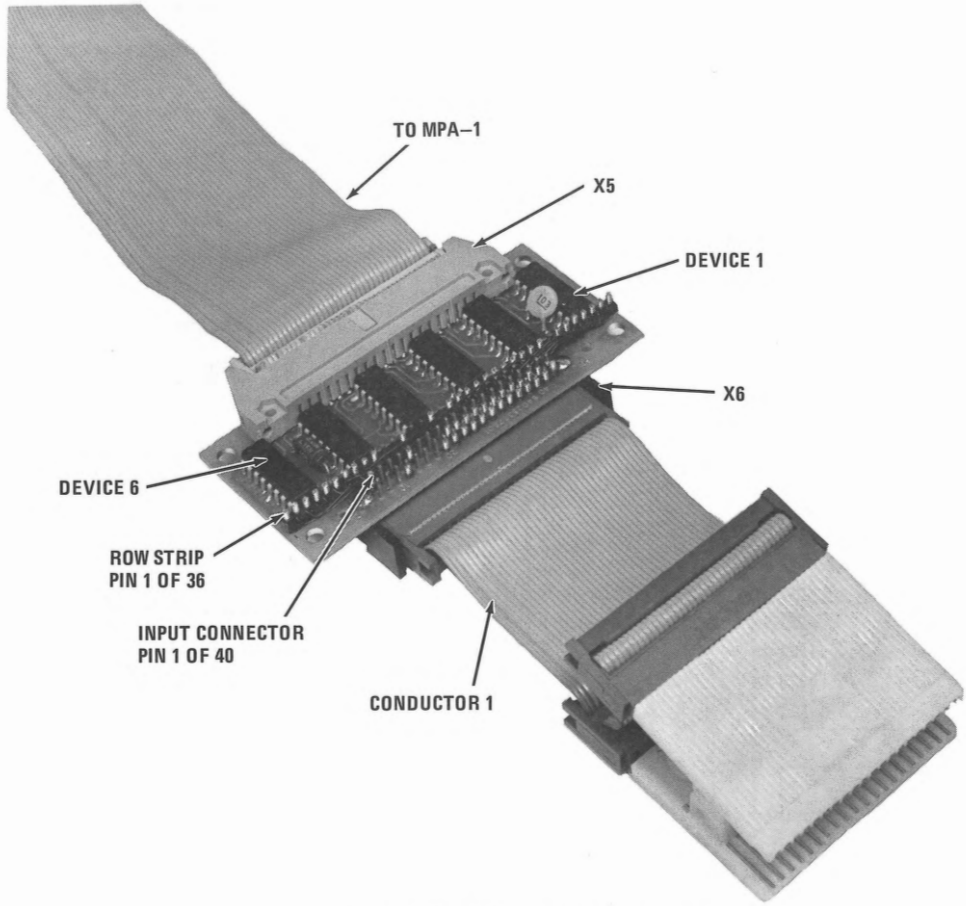


Figure 37. 6800/8080 Probe Buffer

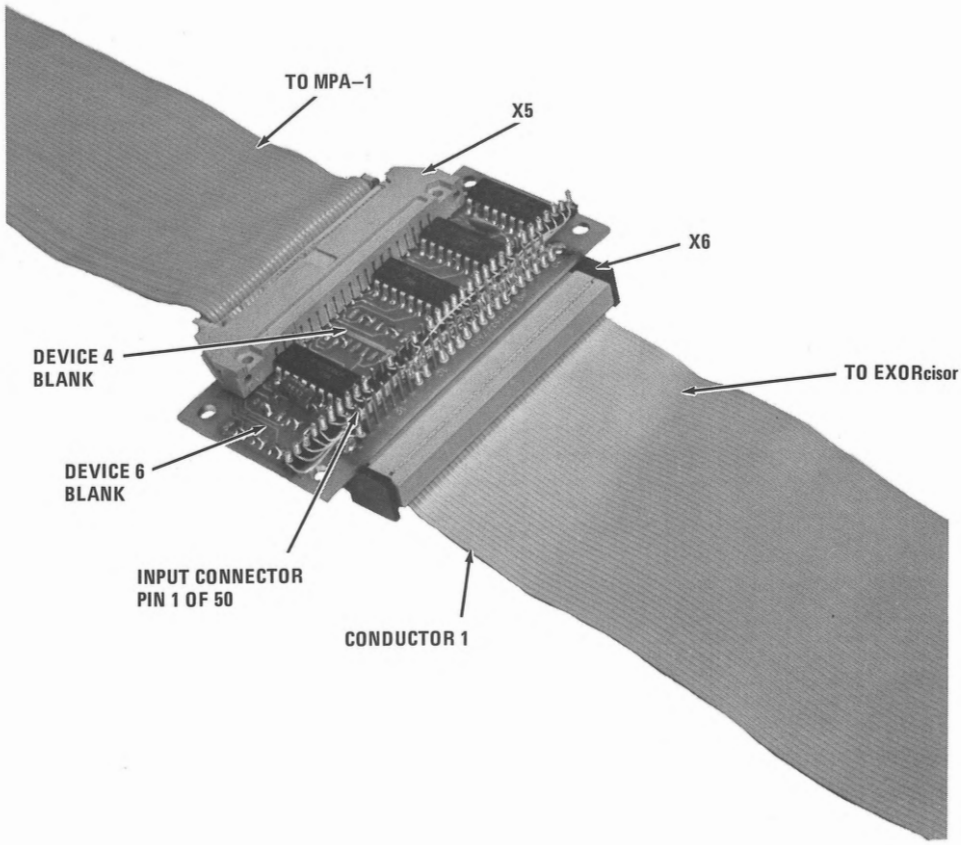
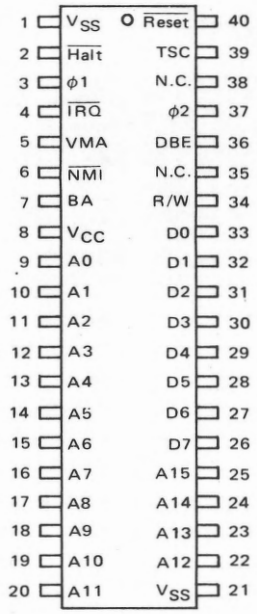
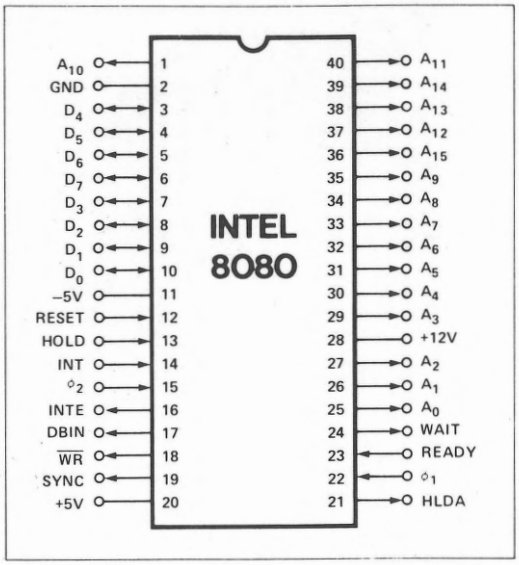


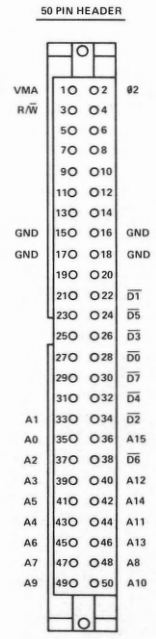
Figure 38. EXORcisor Probe Buffer



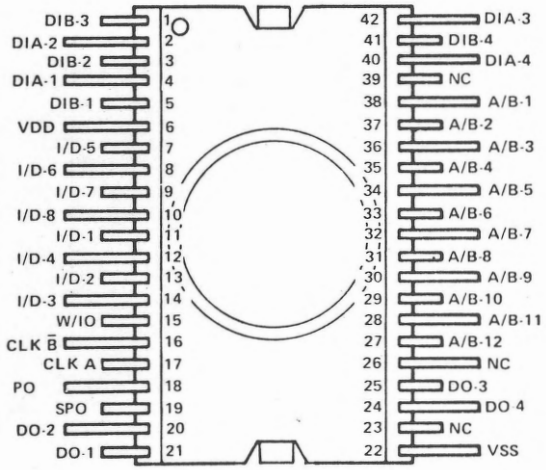
MOTOROLA M6800



INTEL 8080(A)



HEADER ON EXORcisor™



ROCKWELL PPS–4

Figure 39. Processor Pin Assignments

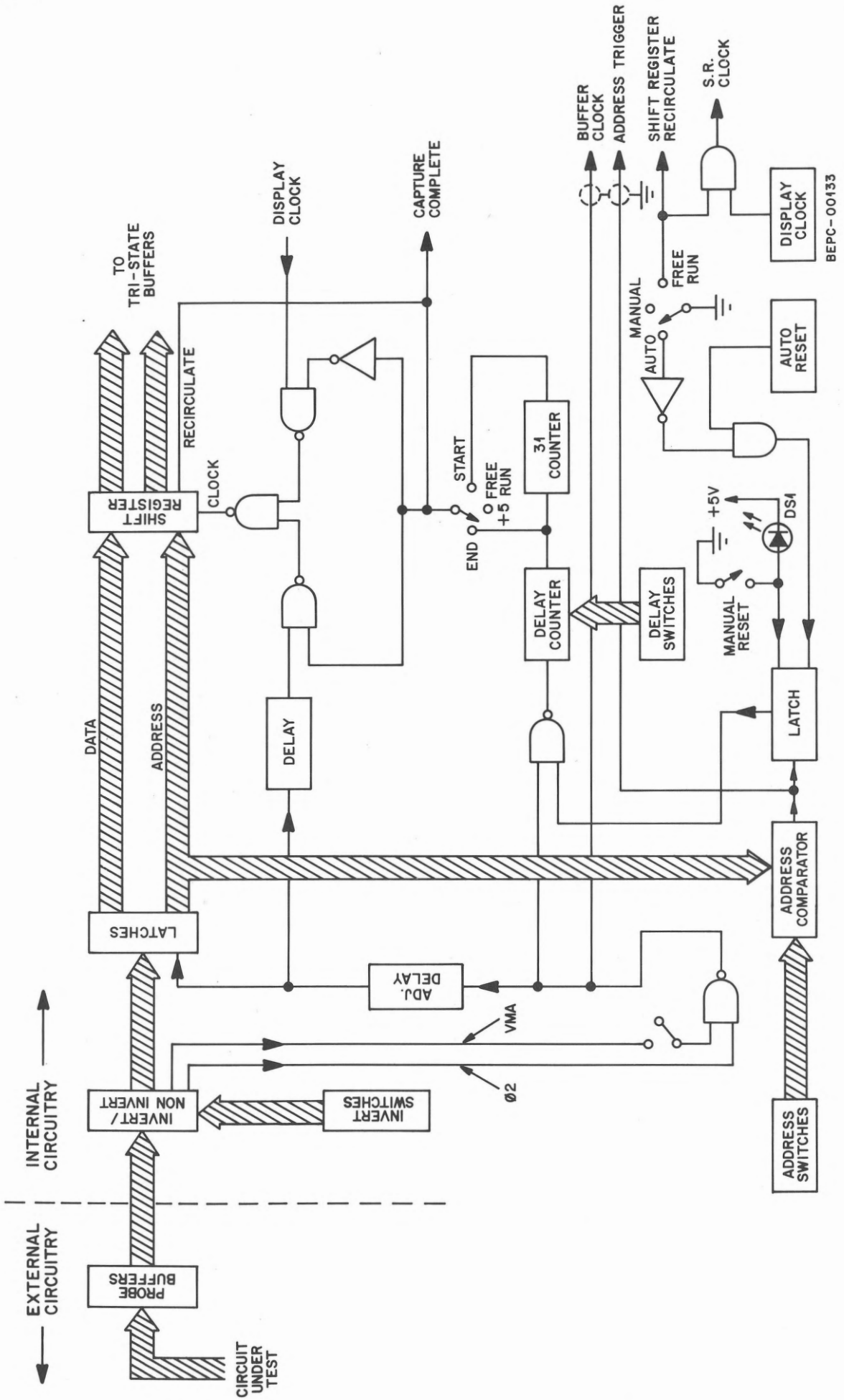


Figure 40. Data Capture Block Diagram

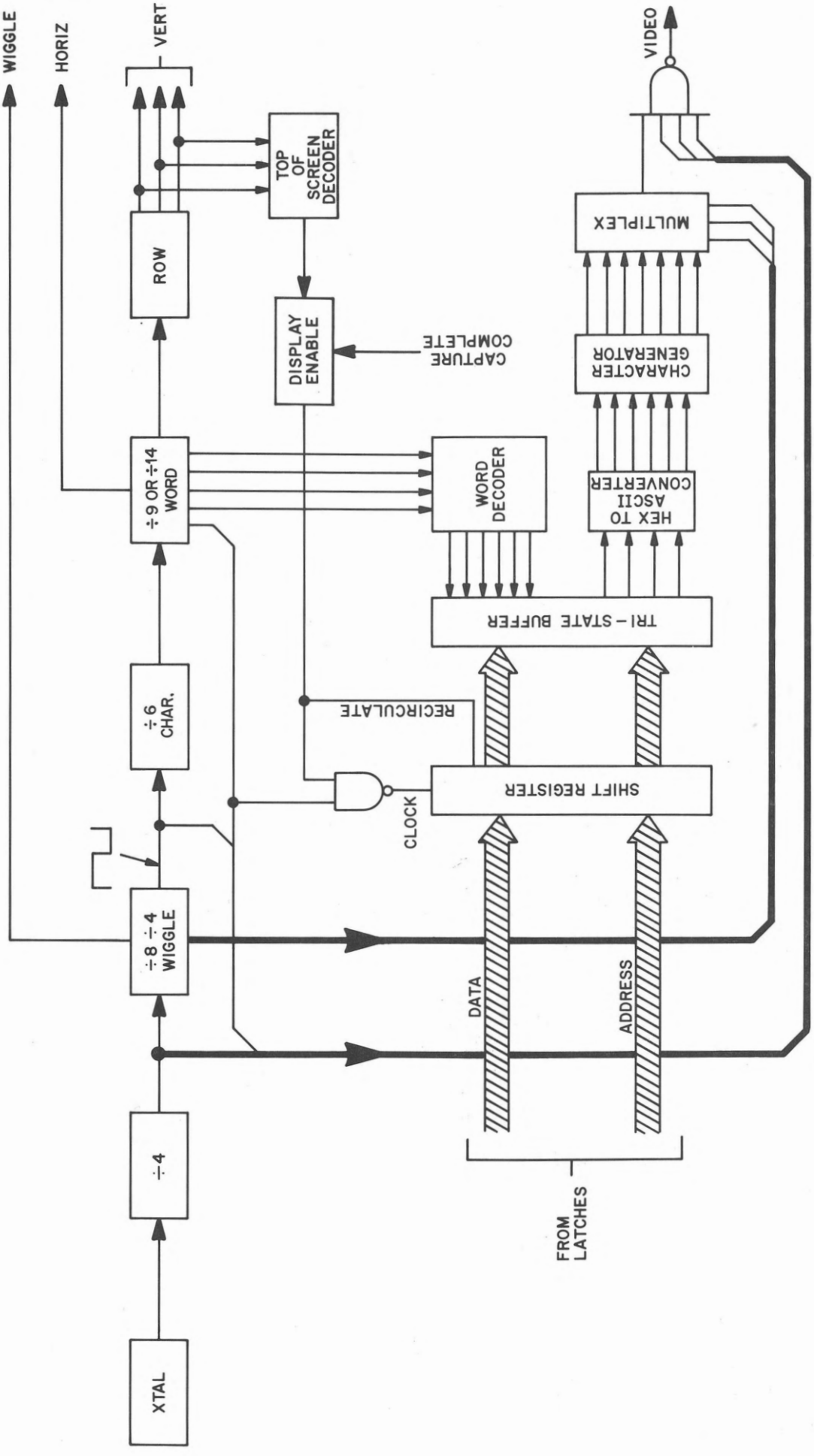


Figure 41. Data Display Block Diagram

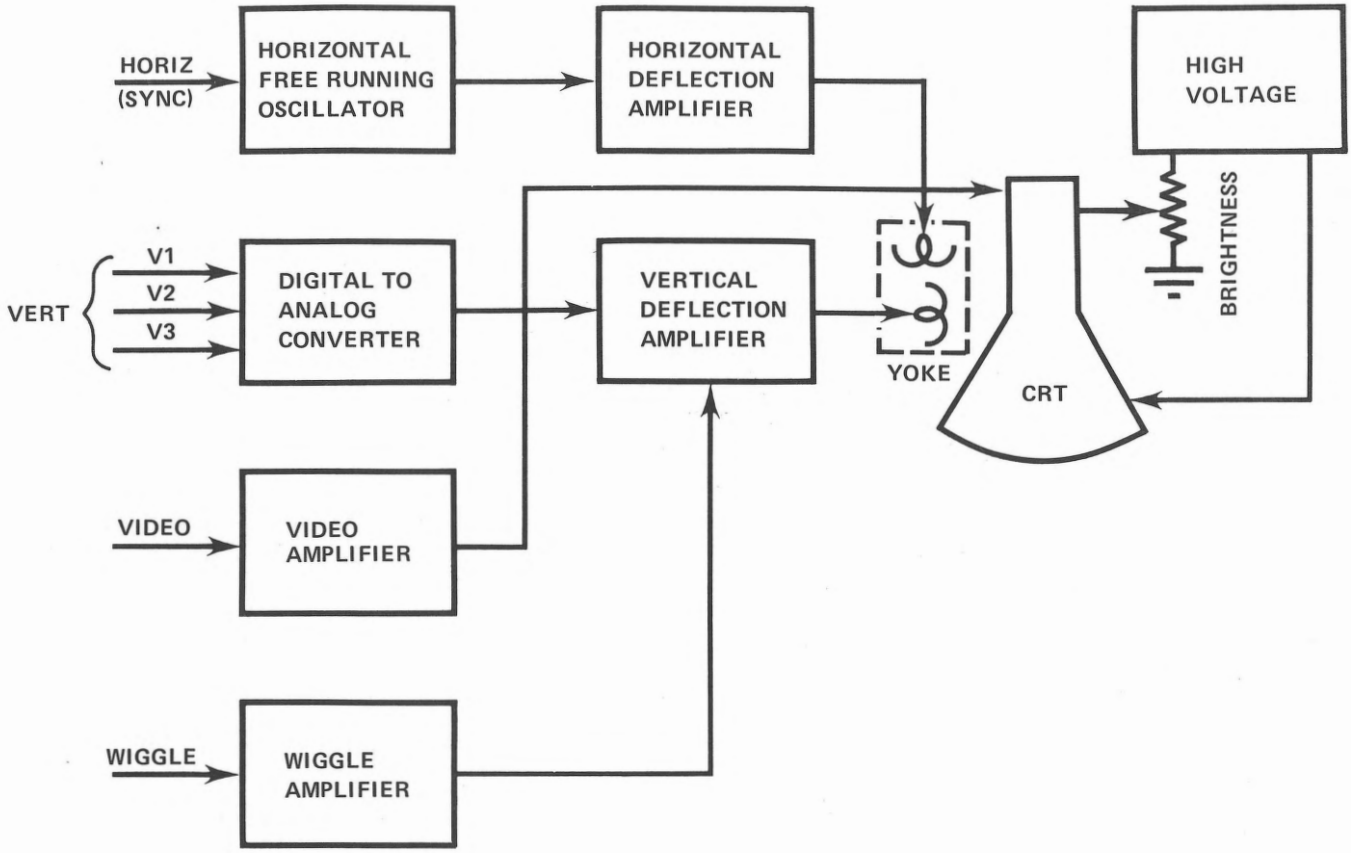


Figure 42. Monitor Block Diagram

REF. NO.	PART NUMBER	DESCRIPTION
POWER SUPPLY		
CAPACITORS: (All values are in microfarads unless otherwise noted.)		
C1,a,b	23R25347A03	14,000, 15V; 14,000, 25V Electrolytic
C2	23S10255A32	470, 50V Electrolytic
C3	23S10255A41	100, 15V Electrolytic
C4	8S10212A90	.15, 250V
C6	23S10255A41	100, 15V Electrolytic
C7	8S10212A90	.15, 250V
C8	23S10218A31	5, 15V Electrolytic
C9	23R25347A02	10,000, 25V Electrolytic
C10	23S10255	100, 15V Electrolytic
C11	8S10212A90	.15, 250V
C12, 13,14	21S180E60	.01, 50V, Disc.
DIODES/RECTIFIERS:		
D1–3	48S191A05	A05 Rectifier
D4	48S10641D91	Zener 9.1V
D5,6	48S191A10	Silicon Rectifier
D7	48S10641D43	Zener 4.3V 1N5231
D8	48S10641D51	Zener 5.1V 1N5239
D9,10	48S191A05	A05 Rectifier
D11	48S10641D91	Zener 9.1V
TRANSISTORS/SCR		
Q1, 3,5	48S137169	A6G
Q2, 4,6	48R25347A01	RCA 2N6288
SCR1	48S137531	W1W S.C.R.
INTEGRATED CIRCUITS:		
IC1–3	51S10732A01	MC1741PC Operational Amplifier
FUSES:		
F1,3	65S136904	1.6 Amp Slow Blow
F2	65S20404	3.0 Amp 250V Littlefuse No. 312003
F4	65S139424	1.0 Amp
RESISTORS/CONTROLS: (Only special resistors and controls are listed. All others are standard 1/2 watt components).		
R2,12	6S10164B29	820 Ohms 1/2W 5%
R4,14	6S10164B39	3.6K Ohms 1/2W 5%
R6	6S10164A79	1K 1/2W 5%
R8	6S10164B42	5.1K 1/2W 5%
R3,7,13	18D25245A01	1K Potentiometer
TRANSFORMERS:		
T1	25D25239A12	Power
SWITCHES:		
	40R25347A13	Power Switch and Indicator
SOCKETS/CONNECTORS/CABLES:		
P1–3	15S10183A83	Transistor Socket
P4	28R25347A05	20 Pin Header
P5	15-10183A12	Plug Housing, 6 Contacts
P5	15-10183A11	Recpt. Housing, 6 Contacts
	39S10061A13	Contacts for P5
X2	9S10764A07	40 Pin Recpt.
J4	9S10764A06	20 Pin
S1	15S1039A09	Edge Connector for P.C. Board
	30R25347A16	Cable No. 22 Ribbon 3 Cond.
	30R25347A21	Cable No. 28 Ribbon 40 Cond. 18"
MISC.:		
	30-10558A04	AC Line Cord
	42S10122A12	Fuse Clip (2 required per fuse)
	5S10277A04	AC Line Cord Bushing
MONITOR		
CAPACITORS: (All values are in microfarads unless otherwise noted.)		
C1,2	8-10191A38	.1, 10%, 250V
C3	21S139646	.1, 50V
C4,6,14, 17,25	8-10212A90	.15, 10%, 250V
C5,30	23-60496A14	300, 15V Eletrolytic
C7	21S180C17	150pF, 10%, Z5F
C8	8-10191C02	.1, 10%, 250V
C9, 21,26	8-10212A10	1, 10%, 100V
C10	21S180B87	220pF, 10%, X5F
C11,15	8-10191A21	.022, 10%, 160V
C12, 13,18	23-10218A31	5, 15V, Tantalum
C16, 31,32	23-10255A41	100, 16V, Electrolytic
C19	23-10255A38	4.7, 63V, Electrolytic
C20	23-10255A46	22, 40V, Electrolytic
C22,23	8-10212A13	.47, 10%, 250V
C24	8-10212A91	.22, 10%, 250V
C27	23-10255A60	100, 63V, Electrolytic
C28	8R25347A07	.022, 10%, 600V, Mylar
C29	23-10255A19	100, 40V, Electrolytic
RESISTORS/CONTROLS: (Only controls and special resistors are listed. All others are standard components.)		
R35	6S126C63	3.9K 1 Watt 10%
R64,65	6R25347A14	1.8 Ohms 3.25 Watt Wire Wound
R11,44	18D25245A14	500 Ohms Trimpot – Vert. Size, Horiz. Lin.
R27	18D25245A13	4K Trimpot – Horiz. Size
R51	18D25245A15	100K 30% Trimpot – Brightness Limiter
R68	18D25245A23	100 Ohms Trimpot – Vert. Centering
R72	6S125C73	10K, 10%, 1/2W Film
DIODES:		
D1–14	48D67120A11	A11 Diodes
D15	48-10641B13	Zener 13V 1N5243
D16–23	48S134978	D1K Diodes
D24	48-10641D33	Zener 3.3V 1N5226B
TRANSISTORS:		
Q1	48S134937	A1Z
Q2,4, 6,7,8,	48S137172	A6J

REF. NO.	PART NUMBER	DESCRIPTION
11,19		
Q3,5	48S137324	P4C
Q9	48S137169	A6G
Q10	48S137168	P2V
Q12	48S134997	A3K
Q13	48S137368	AW8
Q14	48S137093	A5F
Q15	48S137609	MPS–U51
Q16	48–	A5F – Selected
Q17,18	48S137462	A9Z
TRANSFORMERS/COILS:		
T1	24D25291A01	Flyback Transformer
L1	24D25248A03	Yoke Choke
L2	25D25221A02	Choke Iron Core
	24D25290A01	Yoke Deflection Coil
SOCKETS/CONNECTORS:		
J1,2,3	15R25347A08	Housing, 10 Contact
	39R25347A10	Contacts for J1, 2, 3
J1,2,3	28R25347A09	Header 10 Contact
	9D25241A06	CRT Socket Assembly
	9C67532A07	TO3 Sockets for Q13, 17, 18
MISC.:		
V1	96S252A01	C.R.T. 9" P31
	41-65987A01	Aquadag Spring
	42R25347A12	H. V. Connector – 2nd Anode
	1C25219A02	High Voltage Multiplier

LOGIC BOARD

CAPACITORS:
(All values are in microfarads unless otherwise noted.)

CA, B,C	23S10255A41	100, 16V, Electrolytic
CD	21S10052A58	470pF 5%, 100V Sil Mica
CE	21S10052A56	150pF 5% 500V Sil Mica
CF,CH	21S10052A59	1100pF 5%, 100V Sil Mica
CG	21S10052A57	300pF 5%, 300V Sil Mica
RESISTORS:		
RA	6S10164A15	220 Ohms, 10%, 1 Watt, FC Film
RB	6S10164J58	180 Ohms, 10%, 1/4 Watt, FC Film
RC	6S10164H51	82 Ohms, 5%, 1/4 Watt, FC Film
	6R25347A57	Resistor Pack 15 X 2K Ohms (B1, C1, F1, K5)
	6R25347A58	Resistor Pack 15 X 6.8K Ohms (J4)
DIODES:		
DA, DC,DD	48S134978	Diode D1K
DB	48S10641D51	Zener Diode 5.1V
INTEGRATED CIRCUITS:		
	51R25347A36	I.C. 7400
	51R25347A37	I.C. 7402
	51R25347A38	I.C. 7404
	51R25347A39	I.C. 7408
	51R25347A40	I.C. 7410
	51R25347A41	I.C. 7420
	51R25347A42	I.C. 7430
	51R25347A43	I.C. 7442
	51R25347A44	I.C. 7475
	51R25347A45	I.C. 7486
	51R25347A46	I.C. 7493
	51R25347A47	I.C. 74107
	51R25347A48	I.C. 74123
	51R25347A49	I.C. 74151
	51R25347A50	I.C. 74163
	51R25347A51	I.C. 74188 Programmed ROM
	51R25347A52	I.C. 74193
	51R25347A53	I.C. 2518
	51R25347A54	I.C. 3257
	51R25347A55	I.C. 8097
MISC.:		
	48R25347A56	Crystal 6.912 MHz
S4,7	40R25347A59	Switch Dip Amp 1-435668-8
	11R25347A81	Tape Dip Sw. Amp 4-35682-2
X1	28R25347A64	Header 50 Pin
X2,3	28R25347A18	Header 40 Pin

FRONT AND BACK PANELS

SWITCHES:

S1,2	40R25347A68	Switch – On-Off-On Single Pole
S3	40R25347A69	Switch – On-None-On DPST
S5	40R25347A67	Switch – N.O. Push Button - Momentary
S6	40A25375A01	Switch – 10 Position Rotary
	40R25347A66	Switch – Hexadecimal - Address, Delay
CONNECTORS:		
X1	9R25347A20	Connector 50 Pin, No Cable
X3,4	9S10764A07	Connector 40 Pin, No Cable
	28R25347A63	Header 40 Pin
	9S10549A04	Receptacle – BNC – for Trigger and Clock Outputs
MISC.:		
R50	18D25218A01	Potentiometer – Brightness Control – 100K
	3669224A03	Knob – for Brightness Control
	30R25347A21	Cable – 40 Conductor – No Connectors

PROBE BUFFERS – 6800/8080

MISC.:		
	15R25347A01	Case – for Probe Buffer
	51R25347A24	I.C. 14049 CMOS Buffer
	23S10218A31	Capacitor, 5mfd, 15V, Tant.
	21S131468	Capacitor, .01mfd, 50V, Disc
	29R25347A23	Connector – Pin Row
	28R25347A18	Header – 40 Pin
	28R25347A30	Header – 40 Pin, Wire Wrap, Berg

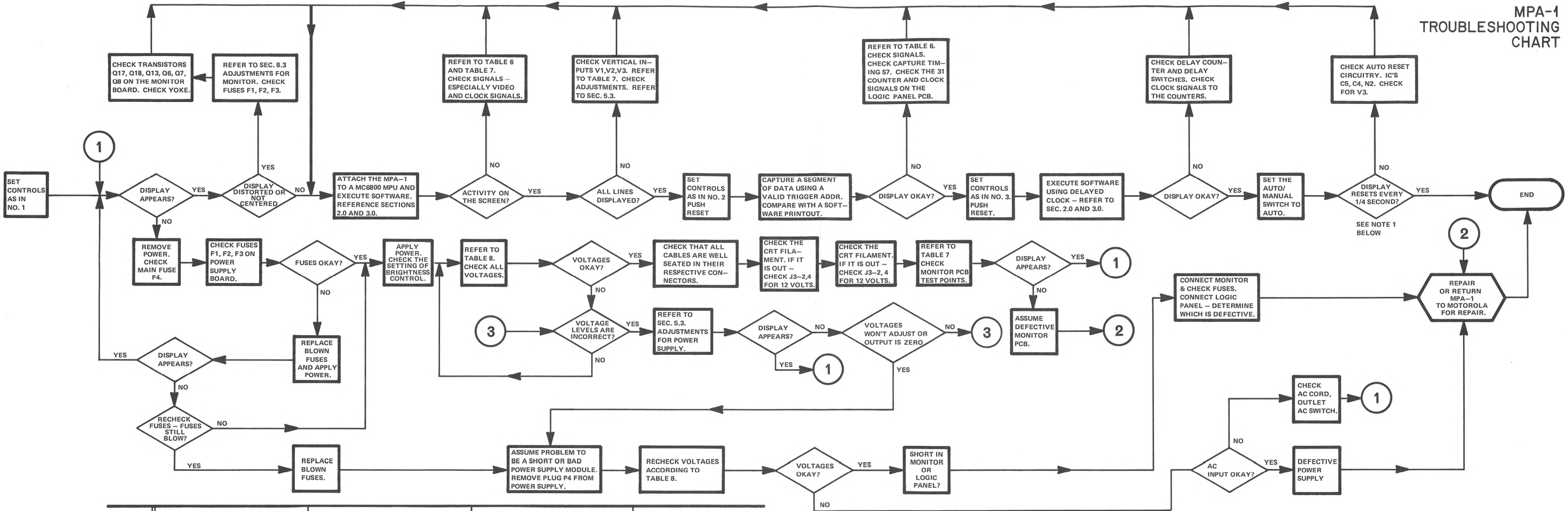
PROBE BUFFER – EXORcisor™

MISC.:		
	15C25367A02	Case – for Probe Buffer
	51R25347A24	I.C. 14049 CMOS
	23S10218A31	Capacitor, 5mfd, 15V, Tant.
	21S131468	Capacitor, .01mfd, 50V, Disc
CONNECTORS:		
	28R25347A18	Header 40 Pin
	28R25347A17	Header 50 Pin, Wire Wrap, Berg
	29R25347A23	Connector Pin Row
	9S10764A05	Connector Recpt. 50 Pin
	30R25347A22	Cable (1ft)

ACCESSORIES

MISC.:		
	9R25347A32	I.C. 40 Pin Test Clip
	30R25347A33	Cable, 40 Conductor, Teflon
	39R25347A34	Contacts for Wire Wrap Posts (40 Required)
	15R25347A35	Housing – for Wire Wrap Contacts (40 Required)

MPA-1 TROUBLESHOOTING CHART


SET CONTROLS AS IN NO. 1
DISPLAY APPEARS?
YES
NO
DISPLAY DISTORTED OR NOT CENTERED
CHECK TRANSISTORS Q17, Q18, Q13, Q6, Q7, Q8 ON THE MONITOR BOARD. CHECK YOKE.
REFER TO SEC. 8.3 ADJUSTMENTS FOR MONITOR. CHECK FUSES F1, F2, F3.
ATTACH THE MPA–1 TO A MC6800 MPU AND EXECUTE SOFTWARE. REFERENCE SECTIONS 2.0 AND 3.0.
ACTIVITY ON THE SCREEN?
REFER TO TABLE 6 AND TABLE 7. CHECK SIGNALS – ESPECIALLY VIDEO AND CLOCK SIGNALS.
ALL LINES DISPLAYED?
CHECK VERTICAL IN–PUTS V1,V2,V3. REFER TO TABLE 7. CHECK ADJUSTMENTS. REFER TO SEC. 5.3.
SET CONTROLS AS IN NO. 2 PUSH RESET
CAPTURE A SEGMENT OF DATA USING A VALID TRIGGER ADDR. COMPARE WITH A SOFT–WARE PRINTOUT.
DISPLAY OKAY?
REFER TO TABLE 6. CHECK SIGNALS. CHECK CAPTURE TIM–ING S7. CHECK THE 31 COUNTER AND CLOCK SIGNALS ON THE LOGIC PANEL PCB.
SET CONTROLS AS IN NO. 3. PUSH RESET.
EXECUTE SOFTWARE USING DELAYED CLOCK – REFER TO SEC. 2.0 AND 3.0.
DISPLAY OKAY?
CHECK DELAY COUN–TER AND DELAY SWITCHES. CHECK CLOCK SIGNALS TO THE COUNTERS.
SET THE AUTO/ MANUAL SWITCH TO AUTO.
DISPLAY RESETS EVERY 1/4 SECOND?
CHECK AUTO RESET CIRCUITRY. IC'S C5, C4, N2. CHECK FOR V3.
SEE NOTE 1 BELOW
END
REMOVE POWER. CHECK MAIN FUSE F4.
CHECK FUSES F1, F2, F3 ON POWER SUPPLY BOARD.
FUSES OKAY?
REPLACE BLOWN FUSES AND APPLY POWER.
DISPLAY APPEARS?
RECHECK FUSES – FUSES STILL BLOW?
REPLACE BLOWN FUSES.
APPLY POWER. CHECK THE SETTING OF BRIGHTNESS CONTROL.
REFER TO TABLE 8. CHECK ALL VOLTAGES.
VOLTAGES OKAY?
CHECK THAT ALL CABLES ARE WELL SEATED IN THEIR RESPECTIVE CON–NECTORS.
CHECK THE CRT FILA–MENT. IF IT IS OUT – CHECK J3–2,4 FOR 12 VOLTS.
CHECK THE CRT FILAMENT. IF IT IS OUT – CHECK J3–2, 4 FOR 12 VOLTS.
REFER TO TABLE 7 CHECK MONITOR PCB TEST POINTS.
DISPLAY APPEARS?
ASSUME DEFECTIVE MONITOR PCB.
VOLTAGE LEVELS ARE INCORRECT?
REFER TO SEC. 5.3. ADJUSTMENTS FOR POWER SUPPLY.
DISPLAY APPEARS?
VOLTAGES WON'T ADJUST OR OUTPUT IS ZERO
ASSUME PROBLEM TO BE A SHORT OR BAD POWER SUPPLY MODULE. REMOVE PLUG P4 FROM POWER SUPPLY.
RECHECK VOLTAGES ACCORDING TO TABLE 8.
VOLTAGES OKAY?
SHORT IN MONITOR OR LOGIC PANEL?
CONNECT MONITOR & CHECK FUSES. CONNECT LOGIC PANEL – DETERMINE WHICH IS DEFECTIVE.
REPAIR OR RETURN MPA–1 TO MOTOROLA FOR REPAIR.
AC INPUT OKAY?
CHECK AC CORD, OUTLET AC SWITCH.
DEFECTIVE POWER SUPPLY
1
2
3

CONTROL SETTINGS FOR TESTS	1	2	3	
	AUTO/MANUAL : FREE RUN	AUTO/MANUAL : MANUAL	AUTO/MANUAL : MANUAL	REFER TO SECTION 2 AND 3 FOR OPERATION ASSISTANCE AND EX–AMPLES. TABLES 6, 7, 8 ARE LOCATED IN SECTION 5.4
	START/END : FREE RUN	START/END : START	START/END : START	
	S3 : Ø2 • VMA	S3 : Ø2 • VMA	S3 : Ø2 • VMA	
	S6 : 6800	S6 : 6800	S6 : 6800	
	S7 : 6800 TIMING	S7 : 6800 TIMING	S7 : 6800 TIMING	
	ADDRESS : N/A	ADDRESS : VALID PROGRAM ADDRESS	ADDRESS : VALID PROGRAM ADDRESS	
	DELAY : N/A	DELAY : 0000	DELAY : DESIRED CLOCK DELAY	

NOTE 1: PROGRAM MUST BE IN A LOOP USING THE TRIGGER ADDRESS.

* REFER TO SECTION 5.5 – FACTORY REPAIR

Figure 43
MPA–1 Troubleshooting Chart

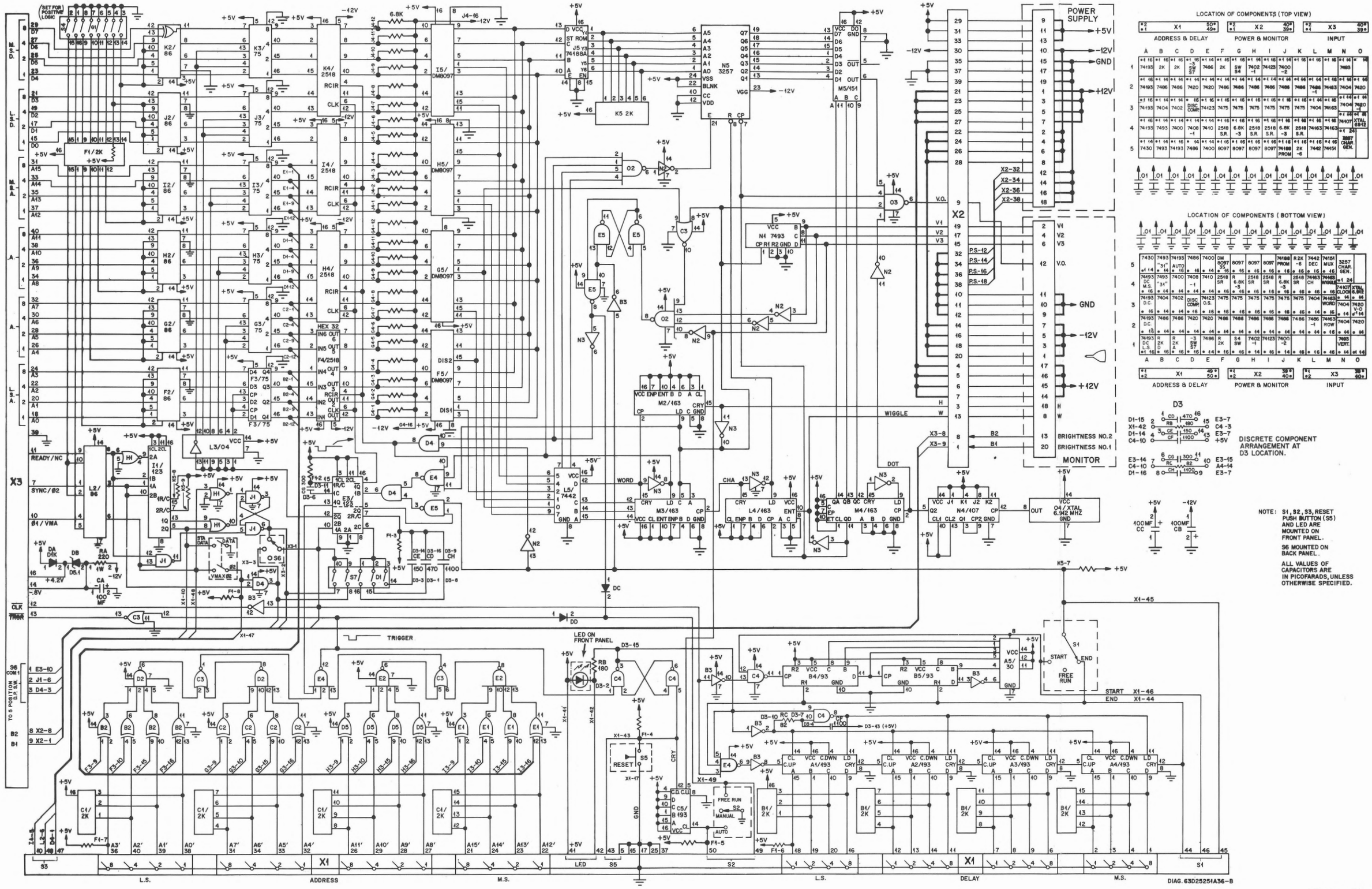


Figure 44
Logic Board Schematic

NOTES:
UNLESS OTHERWISE SPECIFIED:
CAPACITOR DECIMAL VALUES ARE IN MF, ALL OTHERS ARE IN PF. RESISTORS ARE 10% 1/4W.

1. VOLTAGES AND WAVEFORMS SHOWN ARE FOR REFERENCE ONLY, AND VARY WITH CONTROL SETTINGS AND INPUT SIGNALS.
2. ALL VOLTAGE AND WAVEFORM MEASUREMENTS ARE ± 10% AND TAKEN WITH HIGH IMPEDANCE DVM OR WIDE-BAND OSCILLOSCOPE REFERENCED TO CIRCUIT GROUND.
3. ALL WAVEFORM PERIODS OF TIME REFER TO 1 CYCLE OR PULSE. ALL VOLTAGE MEASUREMENTS TAKEN WITH D.V.M. WITH ALL INPUT SIGNALS PRESENT.

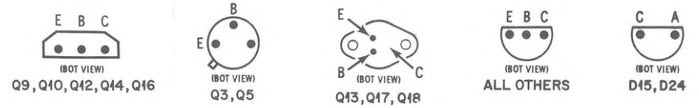


Figure 45
Monitor Board Schematic

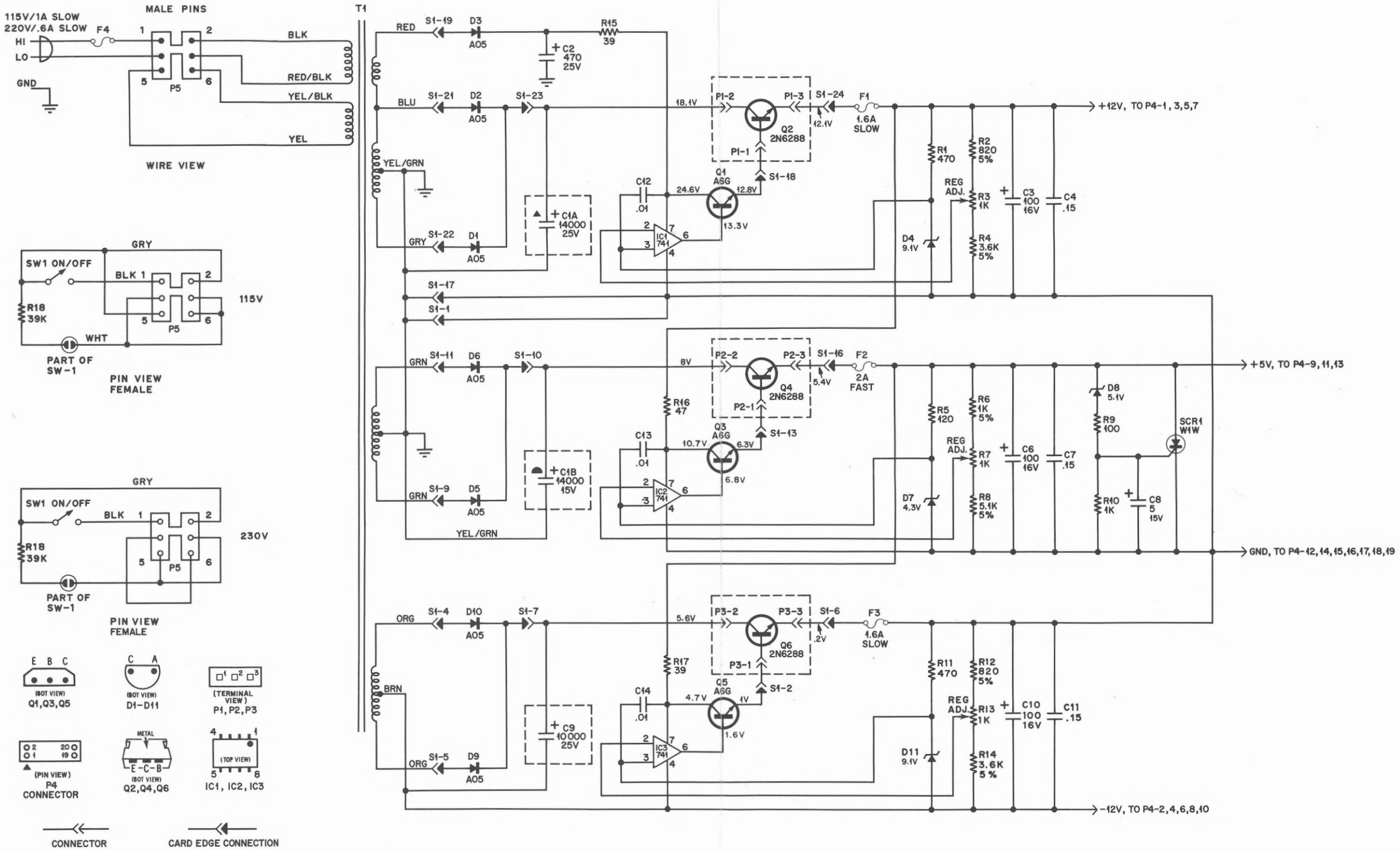
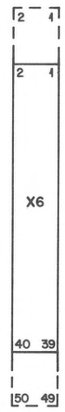


Figure 46
Power Supply Schematic

DIAG. 63D25251A42-A

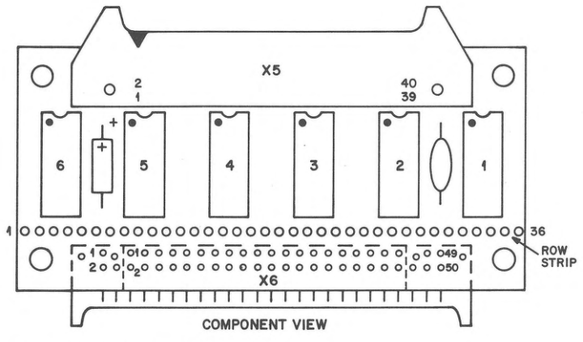
TABLE : 10

FUNCTION	ROW STRIP	STYLE A 40 PIN HEADER 6800	STYLE A 40 PIN HEADER 8080	STYLE B 50 PIN HEADER EXORCISOR*
GND	1	ROW STRIP 7	ROW STRIP 7	15
D5	2	26	7	24
D6	3	28	9	38
D7	4	30	11	30
D2	5	20	15	34
D4	6	24	5	32
GND	7			16
SYNC/Ø2	8	8	37	2
GND	9	1	3	17
Ø1/VMA	10	9	38	1
	11			
READY	12	40	36	18
D1	13	18	17	22
	14			
	15			
D3	16	22	13	26
	17			
D0	18	16	19	28
A4	19	25	22	43
A0	20	17	32	35
A1	21	19	30	33
A5	22	27	20	41
A2	23	21	28	37
A3	24	23	24	39
A7	25	31	16	47
A6	26	29	18	45
A15	27	32	10	36
A8	28	33	14	48
	29			
A9	30	35	12	49
A10	31	37	1	50
A12	32	38	8	40
A13	33	36	6	46
A11	34	39	2	44
A14	35	34	4	42
GND	36	40	3	18
WIRE COLOR		BLK	RED	WHT

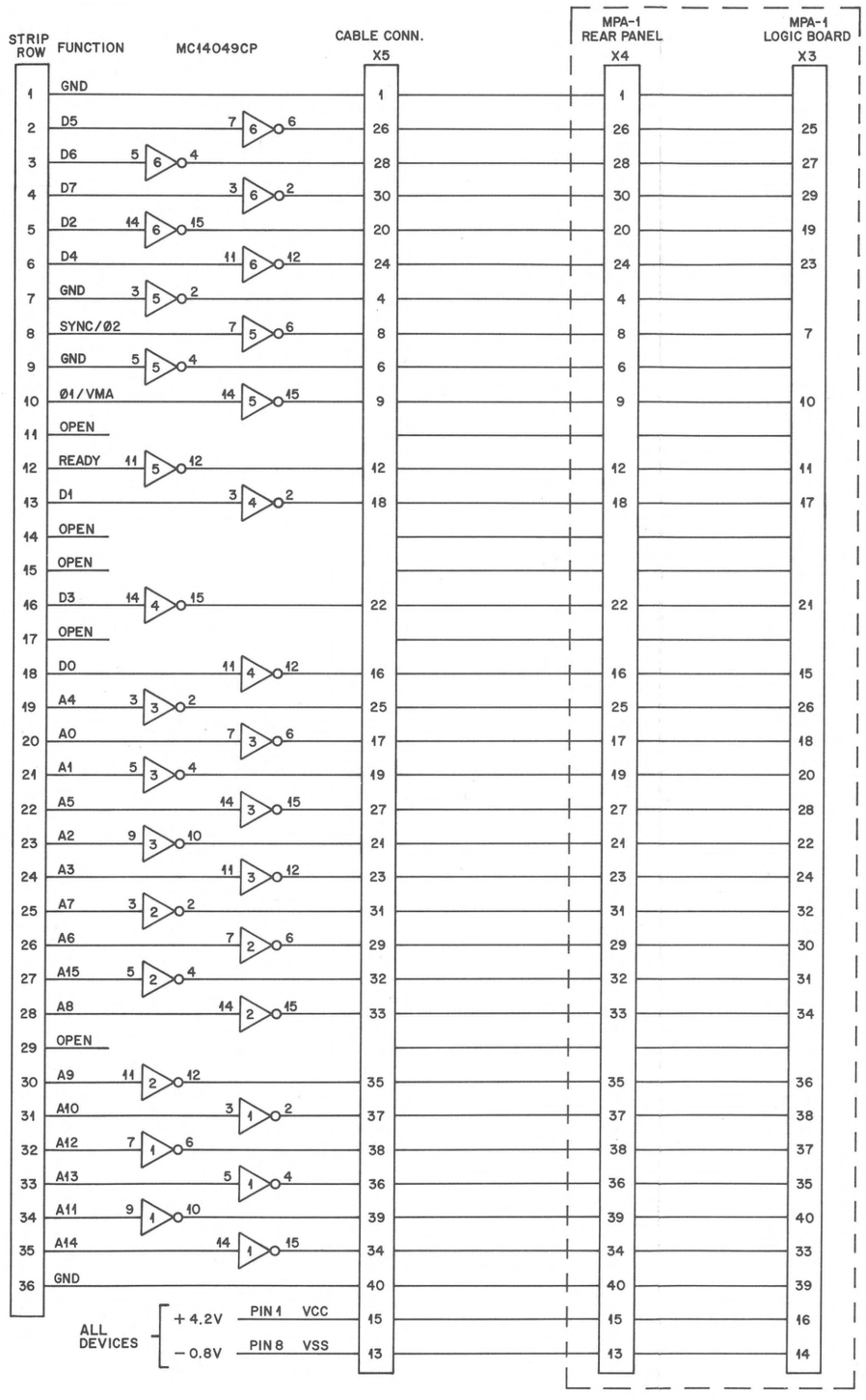


FULL LINE : STYLE A

DOTTED LINE : STYLE B



NOTE : OPEN GATES TIED TO LOW LEVEL



NOTES : 1 * PROBE FOR EXORCISER

A. DO NOT INSERT I.C. NUMBER 4 & 6

B. INSTALL JUMPERS:

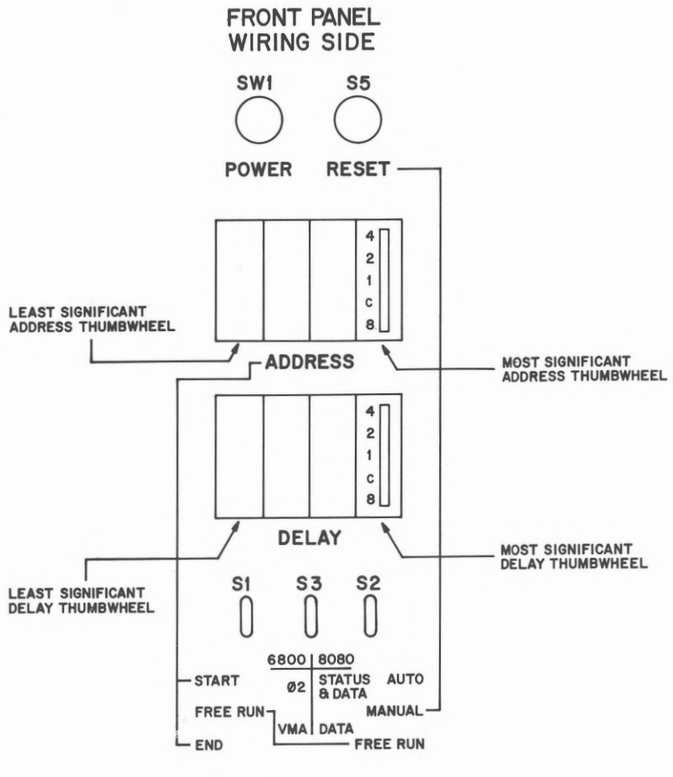
FROM I.C.#	PIN #	TO I.C.#	PIN #
4	2	4	3
4	11	4	12
4	14	4	15
6	2	6	3
6	4	6	5
6	6	6	7
6	11	6	12
6	14	6	15

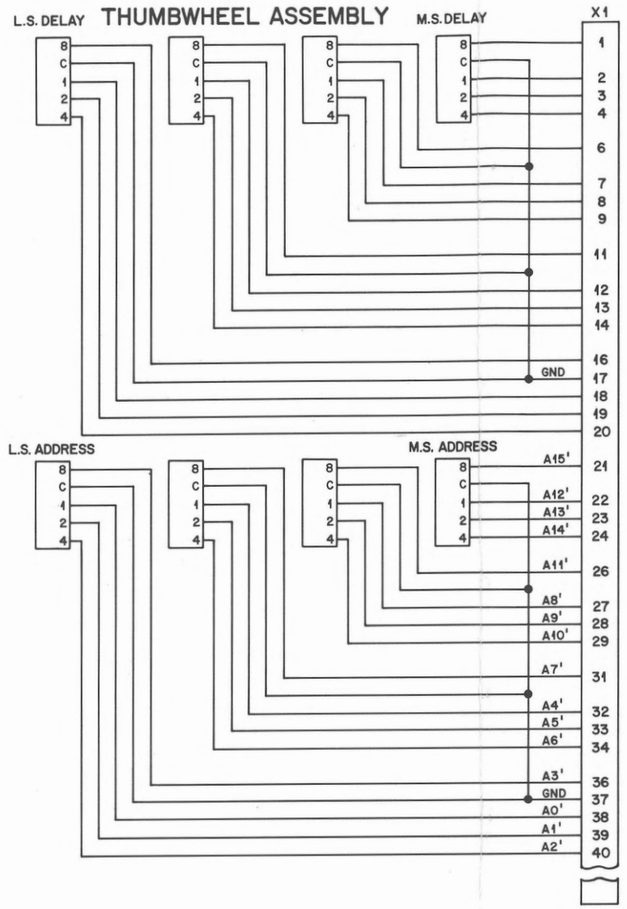
2. UNUSED GATE INPUT TIED TO LOW LEVEL.

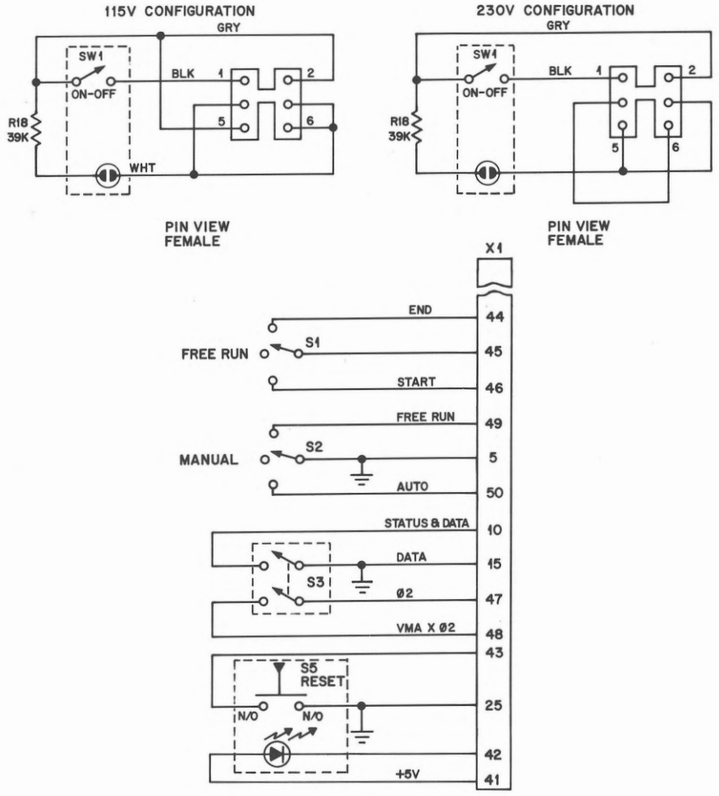
I.C.#	PIN #	I.C.#	PIN #
1	11	4	9
2	9	5	3
4	5	5	9
4	7	6	9

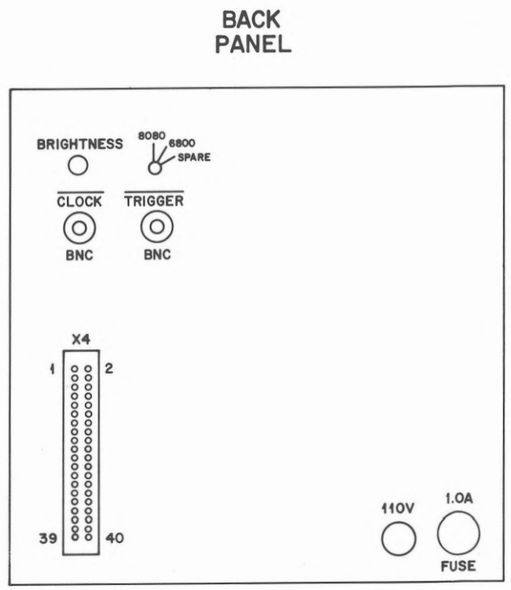
DIAG. 63D25251A49-B

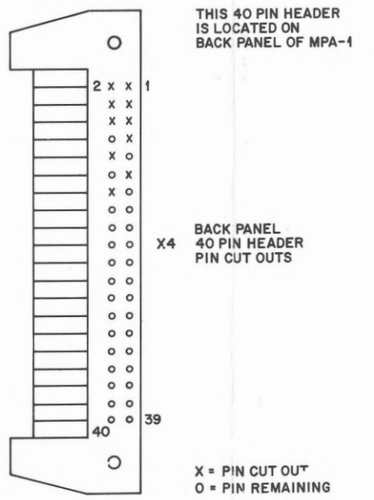
Figure 47
Probe Buffer Schematic 51











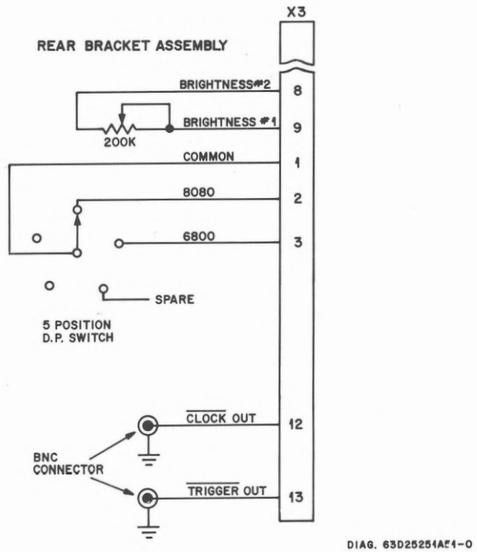


Figure 48
Front and Back Panel Schematic

MOTOROLA
Data Products